HARDWARE DESIGN SPECIFICATION

i-data international confidential

| in margin marks changes from revision 0.00

Table of contents

1. Document log.

Date	Init	Revision	Changes
981221	LCH	1.01	VPN BOX Specification
990407	BKS	0.10	Modified above as a template for VPN Pro product
990419	JSL	0.11	
990611	JSL	1.00	First release.
990701	JSL	1.01	Added: Compression, Phy signal switch, 66MHz PCI, 2 Harddisks.
000407	JSL	1.03	Memmap + interrupt controller
000413	JSL	2.00	PCB Changed.
000531	LCH	2.01	Soft Reset register added.
000619	LCH	2.02	Mem. Map updated with 64Mbyte SDRAM for SafePipe 200
001020	JAL	2.03	Register for flash program enable included in doc
001024	SIP	2.04	Register 4 byte 0 bit 4-7 show the CPLD code version. LED0-LED2 is defined for WAN (ACT, CON and Link). Revision is added as a custom field in Properties. The date is now the field LastSaved. To update fields use “select all” and then press F9. This must be repeated in header, footer and body???

2. General

This document specifies and defines the function of the VPN Pro BOX.
The VPN Pro BOX is used as the common HW platform for both the Masquerade Pro and the SafePipe 200 products, in the following referred to as VPN Pro BOX

The primary functions of the Masquerade Pro are:
- Firewall
- Mail-server
- Web-server.
- Access to two LANs (10/100Base-TX).
- V.35 and X.21access
- PCI sockets for 3 standard PCI Card

The primary function of the SafePipe 200 is to provide a secure and private communication path over the Internet either between two LAN’s or between a LAN and a Remote PC.
The main features of the safePipe includes:
- Access to two LANs (10/100Base-TX).
- Routing
- V.35 and X.21 access
- Encryption
- Authentication
- Internet Key Exchange (IKE)
- PCI sockets for 3 standard PCI Card (1slot reserved for HW VPN functionality)

2.1 Document reference

[1] Am79C972 Datasheets rev B
Enhanced 10/100 Mbps PCI Ethernet Controller
[2] VRC5074 System Controller Chip
[3] VR5000 64-bit Processor

[5] Fujitsu Flash Memory databook
[6] PCI Local Bus Specification
Revision 2.1, June 1, 1995.
[8] Picvue Electronic LCD module databook.
[9] MIPS R5000 Microprocessor, Technical Backgrounder
[10] Address Filter Specification.
[11] IntCtr_EAF Device document, IDEF (DMA Controller)

Overview

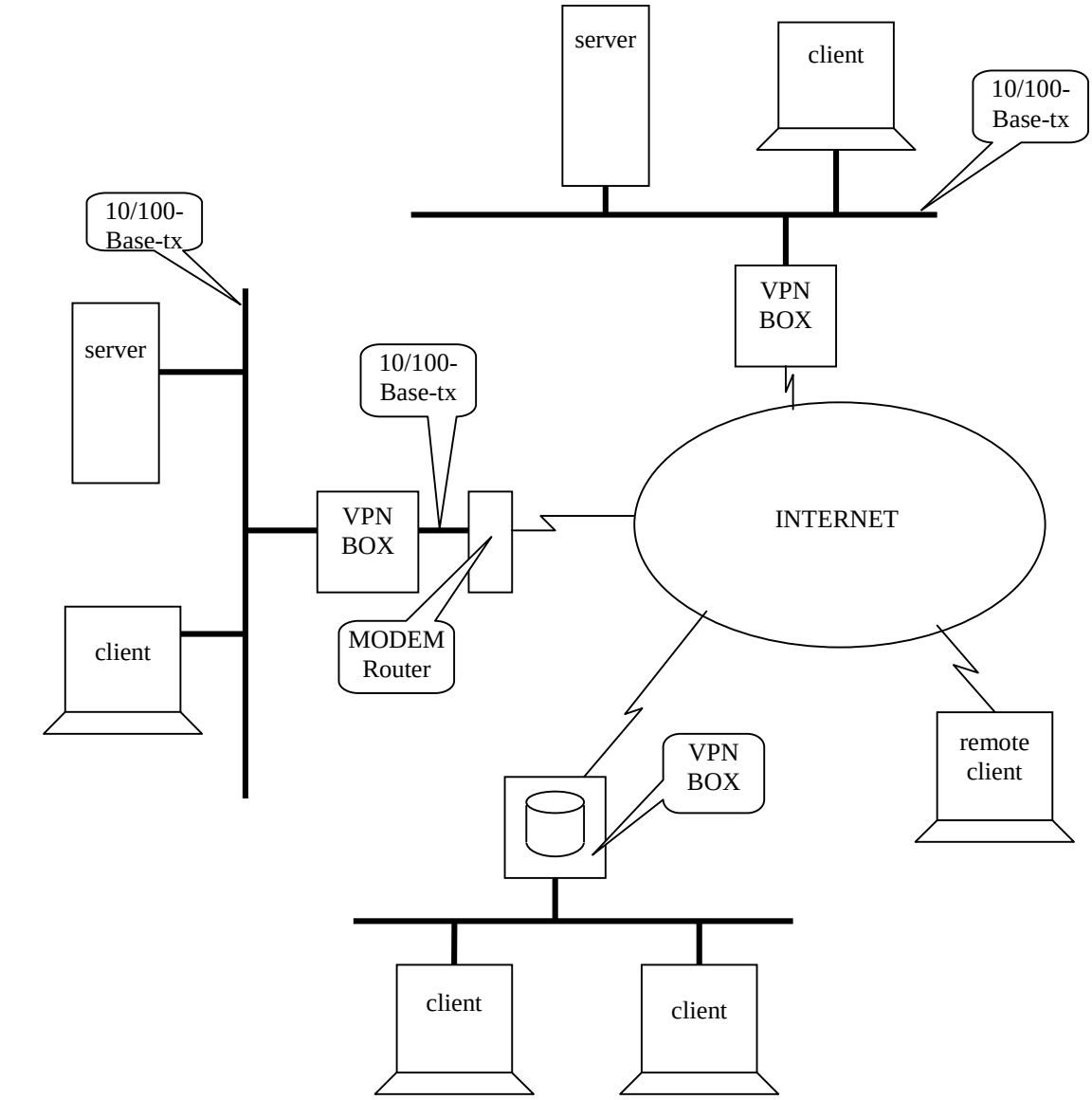
Project name:	<DCG Project name>		
Basis product:	<MOW Basis Product Name>	<S-number>	<Comp number>
Variants:	<MOW Basis Product Name>	<S-number>	<Comp number>

2.2 Abbreviations

IPSec	IP Secure
LAN	Local Area Network
VPN	Virtual Private Network
IKE	Internet Key Exchange
HW VPN	In this context a PCI board with HW accelerated authentication, en/decryption and compression/decompression

3. Product Description

The VPN Pro BOX is a stand-alone unit intended to provide a secure communication path between two LANs or between a LAN and a Remote Client. The figure below shows the environment for the VPN Pro BOX



3.1 Masquerade/safePipe Family

Masquerade II (up to 100 users).
Masquerade Pro *) (up to 500 users).

Safepipe 100
Safepipe 200 *)

*) This document.

3.2 Masquerade Pro/SafePipe 200 Sales Estimates

Price and quantity estimates for the Masquerade Pro and SafePipe 200 Pro products are.

	Masquerade Pro		SafePipe 200	
	Quantity	**End User Price**	**Quantity**	**System Price**
1999	300	6000 $	50	12.000 $
2000	>5,000	3000 $	1,000*	6.000 $
2001	>20,000	1500 $	2,000*	3.000 $

* These quantities do not include OEM.

3.3 Masquerade Pro/safePipe200 Highlights

- All-in-one solution - no other equipment needed
- Unmatched Ease-of-use - 10 Minutes installation
- Strong security
- Local language
- World Wide Web-based configuration interface
- Secure Internet Access - Built-in strong Firewall
- Electronic Mail Server
- World Wide Web Server
- LAN and WAN Connectivity
- Native V.35 and X.21 support
- Virtual Private Networking (VPN)
- T3/E3 connectivity with additional PCI card
- HW assisted en/decryption and authentication at wire speed

3.4 Specifications

3.4.1 Masquerade Pro Specifications

- Very stable Linux based operating system
- WAN connectivity via ISDN, V.35 or FR
- LAN connectivity via 10/100 Mbit/s Ethernet
- Web and Mail Server with full integration with existing mail clients
- Strong Firewall and IPSec-based VPN concept (128 bit encryption)
- Hardware support for FR

3.4.2 SafePipe 200 Specifications

- Exchange Data securely between Branches or Offices.

- Makes a secure “tunnel” between two Systems or Networks
- Remote Access - using the Internet to access the LAN
- Full IPSec (The VPN standard)with strong Triple-DES encryption
- Quality of Service (QoS) support via IPv6
- 10 Minutes Installation and unmatched Ease-Of-Use
- All-in-One solution - No other equipment is needed
- Strong security concept - Strong Firewall and VPN

3.5 HW configurations

The table below defines the 3 hardware configurations:

		PCI Slots	Enclosure	V.35/ X.21	Onboard Comp./Decomp.	Onboard Crypt.	Hard Disk
1	Masquerade Pro	1	1U	Yes	Yes	No	Yes
2	SafePipe 110	1	1U	No	Yes	Yes	No
3	SafePipe 200	3	2U	No	No	No	No

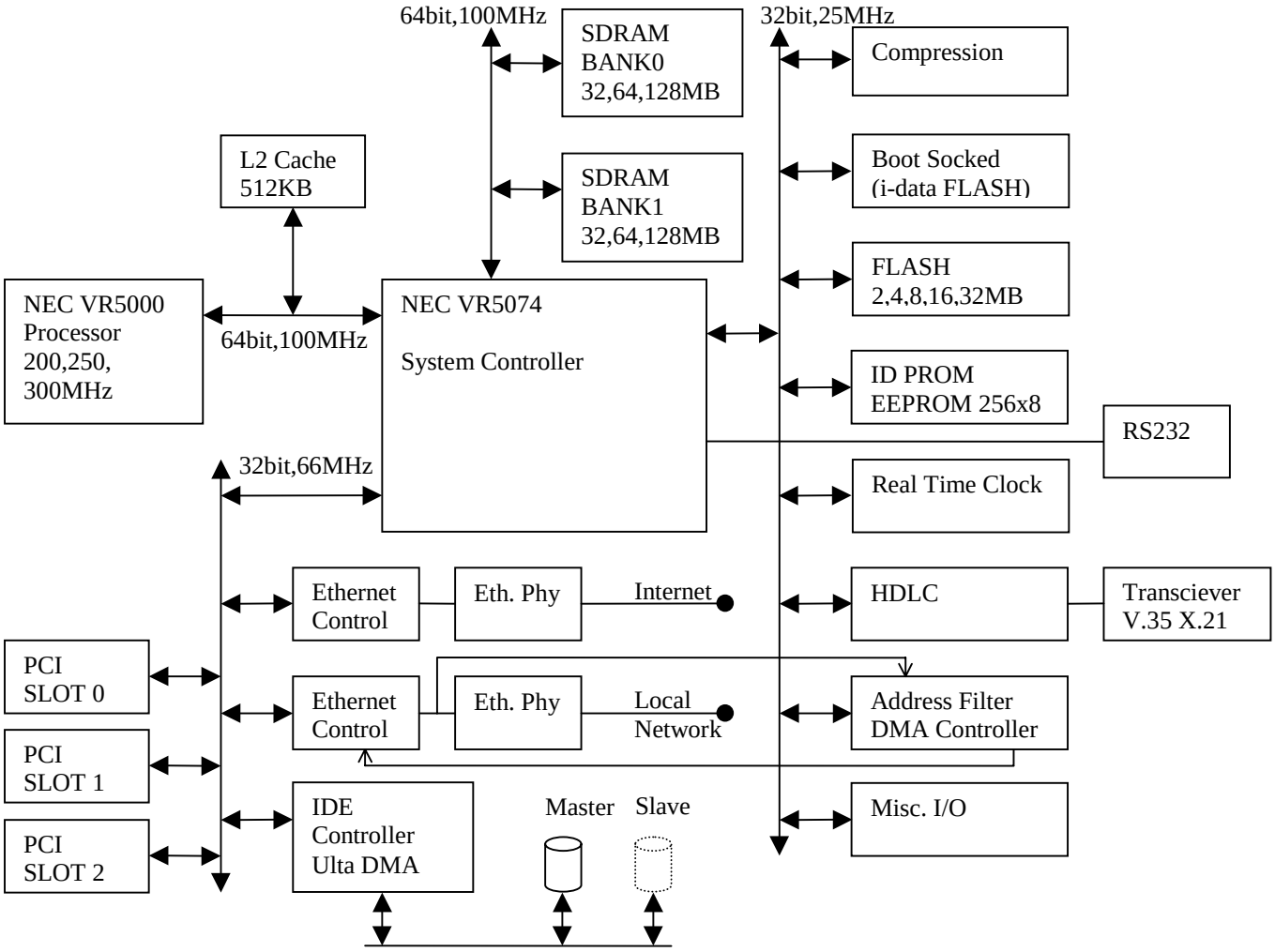
As may be seen from the table or on the following block diagrams the Large Masquerade Pro is the root design. SafePipe 200 and Small Masquerade Pro are both subsets of the Large Masquerade Pro.

1. Masquerade Pro has all the Masquerade software installed. This includes firewall, mail-server and web-server.
2. The Safepipe 110 is a subset of the SafePipe 200.
3. The pure SafePipe 200 with hardware accelerated encryption/decryption.
   HW encryption/decryption is achieved by mounting a PCI board with 2 Ethernet controllers and address filter on-board.

4. Hardware Description

Now the hardware design will be defined. The following subsections show the overall functional blocks and interconnections. Detailed descriptions of implementation and use are explained, and any interfaces are described.

4.1 System Block Diagrams



The figure above shows the basic structures and functional blocks of the design. A System Controller implements a LOCAL BUS for processor peripherals, and a PCI BUS for system peripherals.

The Masquerade Pro motherboard will have following interfaces:

- A 10/100 Mbps Ethernet interface to the internal net with HW filtering.
- A 10/100 Mbps Ethernet interface towards the Internet. This interface implies that an external Modem or similar is connected between the Ethernet and Internet.
- A V.35 / X.21 interface towards the Internet. This interface implies that an external Modem is connected between the SafePipe 200 and the Internet.

When the Motherboard is used in the SafePipe 200 configuration the following components are removed:
- Hard Disc Control
- Compresion

Note. Even though the block diagram shows 3 PCI slots only 2 are available. One slot is always occupied by the HW accelerated VPN functionality
- Compression/decompression
- En/decryption
- Authentication

In the Safepipe 110 configuration the PCI board for compression/decompression and en/decryption would be replaced with a onboard en/decryption chip.

4.2 Functional Description

Divided into subsections explaining the circuit blocks shown in the above System Block Diagram.

4.2.1 MIPS CPU

The mPD30500 (VR5000) is a high-performance, 64-bit RISC (Reduced Instruction Set Computer) type microprocessor employing the RISC architecture developed by MIPS. The instructions of the VR5000 are compatible with those of the VR3000™ series and VR4000™ series and higher, and completely compatible with those of the VR10000™. Therefore, present applications can be used as they are. [3]

VR5000 Processor Characteristics [3]
- Employs 64-bit MIPS-based RISC architecture
- High-speed processing
  - 2-way super scalar 5-stage pipeline
  - 8.3 SPECint95, 8.3 SPECfp95, 423 MIPS @300MHz
- High-speed translation buffer mechanism (TLB) (48 entries)
- Address space Physical : 36 bits
  Virtual : 40 bits
- Floating-point unit (FPU)
  - Sum-of-products operation instruction added
  - Higher operation performance than VR4000 series
- Primary cache memory (instruction/data: 32K bytes each)
- Secondary cache controller
- Operating frequency Internal : 200,250,300 MHz
  External: 100 MHz MAX.
  - External/internal multiple selectable from two to eight
- Instruction set compatible with VR3000 and VR4000 series and higher (conforms to MIPS I, II, III, and IV)
- Supply voltage: 3.3V±5% /1.8V±0.1V

4.2.2 SYSTEM CONTROLLER

The VRC5074 System Controller is a software-configurable chip that directly connects the VR5000 CPU to SDRAM memory, a PCI Bus, and a Local Bus, without external logic or buffering. From the CPU's viewpoint, the controller acts as a memory controller, DMA controller, PCI-Bus host bridge, and Local-Bus host bridge. From the view-point of PCI agents, the controller acts as master and target on the PCI Bus. The controller also has one serial port and four timers. [2]

CPU Interface
- 100 MHz CPU bus.
- Peak block-transfer throughput of 800 Mbytes/sec, maximum sustained throughput of 640 Mbytes/sec.

- Little-endian or big-endian byte order on CPU interface.
- Supports secondary cache.
- 15 interrupt sources, individually enabled and assigned to one of the CPU's seven interrupt inputs.
- Mode data at reset provided by a serial EEPROM or by the controller.
- 3.3V I/O.

Memory Interface

- 100 MHz memory bus.
- Maximum sustained throughput of 800 Mbytes/sec.
- Supports three physical loads per data bit: two SDRAM physical banks and one other (e.g., EPROM, Flash, or buffers Bridging to a secondary memory bus).
- Supports four types of SDRAM with two to four on-chip virtual banks: 256Mb four-bank, 64Mb four-bank, 64Mb two-bank, 16Mb two-bank.
- On-chip bank-interleaving buffers.
- Programmable address ranges for each memory bank.
- On-chip refresh generation.
- 3.3V I /O.

PCI Bus

- Full compliance with PCI Local Bus Specification, Revision 2.1.
- Provisions for 66MHz.
- PCI-Master support, allowing the CPU, DMA, and Local-Bus masters to access targets on the PCI Bus via two programmable PCI Address Windows.
- PCI-Target support, allowing PCI-Bus masters to access to all controller resources.
- Eleven programmable Base Address Register (BAR) windows.
- Optional PCI Central Resource functions:
  - Buffered PCI clock to 5 other PCI devices.
  - PCI clock can be external or derived from CPU clock.
  - Arbitration for the controller and 5 other PCI devices.
  - CPU interrupt control for 5 PCI devices.
- Full PCI Configuration Space.
- 64-bit addressing support for master and target using Dual Address Cycle (DAC).
- Locked cycle (exclusive access) support as master and target.
- Parity generation and checking on address and data cycles.
- Compliant with both 3.3V and 5V PCI signaling.

Local Bus

- 25 MHz or 50 MHz bus (0.25 or 0.50 of system clock).
- Programmable chip-selects for 7 devices plus Boot ROM.
- Arbitration protocols.
- Programmable control-signal relationships and timing:
  - Timing can be fixed or use external Ready signal.
  - 12-bit timer for external Ready signal.
- 3.3V outputs, 5V-tolerant inputs

DMA

- Two DMA channels.
- Block transfers to or from any physical address.
- Transfers initiated by the CPU, a PCI-Bus master, or a Local-Bus master.
- Peak block-transfer throughput of 800 Mbytes/sec, maximum sustained throughput of 640 Mbytes/sec.
- 32 x 8-byte (256-byte) DMA FIFO.
- Two sets of DMA control registers. One set can be programmed while the other performs a transfer.
- Chained transfers—when one transfer completes, another programmed transfer automatically begins.
- Optional hardware handshake signals (REQ#, ACK#, EOT#) if certain chip-selects are not used.

Serial Port (UART)

- Compatible with National Semiconductor's PC16550D UART.

Timers

- 16-bit SDRAM refresh timer.
- 24-bit CPU-bus read timer.
- 32-bit general-purpose timer.
- 32-bit watchdog timer.

All timers are cascadable.

4.2.3 INITIAL BOOT SOCKET

The initial Boot Socket is a socket for a standard i-data 4Mbyte flash module. Preprogramming such a module with boot code and possible some part of or all the application code, it can be inserted into the board and be used as boot memory. When a module is inserted it configures the boot circuit to boot from this memory whereas the onboard flash is mapped into another memory area. Flash module status “inserted” is then visible in the board registers. In this state the defined boot sector in on board flash will be enabled for programming. Flash on the module can not be programmed from the board.

The module voltage is 3.3V

4.2.4 FLASH

The on board FLASH is configured in 2 banks selected by address decoding. When the “initial boot socket” is empty the boot sector is mapped into the boot memory (0.1FC0.0000 and above). The boot memory is write protected and register status shows “no module inserted.

The FLASH is configured as 1, 2, 4, 8 or 16 Mbytes of flash. It’s not upgradable from one size to another.

The PCB layout has 2 banks of 2*16bit devices. The position supports 4Mbit, 8Mbit, 16Mbit or 32Mbit devices all in a tsop package. As they are footprint compatible it then implements:

Bank 0/1	Bank size [Mbyte]
2*2Mbit(128K*16bit)	0.5
2*4Mbit(256K*16bit)	1
2*8Mbit(512K*16bit)	2
2*16Mbit(1M*16bit)	4
2*32Mbit(2M*16bit)	8
2*64Mbit(4M*16bit)	16

The layout is also applicable for simultaneous read, write types of flash (in a tsop package). The preferred selection of flash devices is the AMD/Fujitsu boot sector inherent 3,3V flash devices. These come in 2 versions, one with the included boot sector placed in the beginning and one in the end of the flash. As this boot sector will not be used in this product as boot sector, we will chose the version with the inherent boot sector in the end of the flash address area. When the “initial boot socket” has a module inserted, the module memory is mapped into the boot memory (maximum of 4Mbyte available). Detection of this will enable the on board flash boot sector for programming and in board registers show status of a module inserted.

Flash memory is also given a permanent memory location. This is sw programmable through registers in the System Controller, see 4.3. To be able to program any part of the flash, additional write protection (in board registers) must be disabled. This also goes for boot sector programming when a module is inserted.

The boot address will not be aligned to the top/bottom if the FLASH is lager than 4Mbyte.

The module voltage is 3.3V

4.2.5 SDRAM

The system Controller supports 2 bank of SDRAM. Each bank has 4 16bit SDRAM devices. The banks support 64 and 256Mbit devices, and they are not upgradable from one size to another. The possible configurations are:

SDRAM device [Mbit]	Bank0 [Mbyte]	Bank1 [Mbyte]
64	32	-
64	32	32
256	128	-
256	128	128

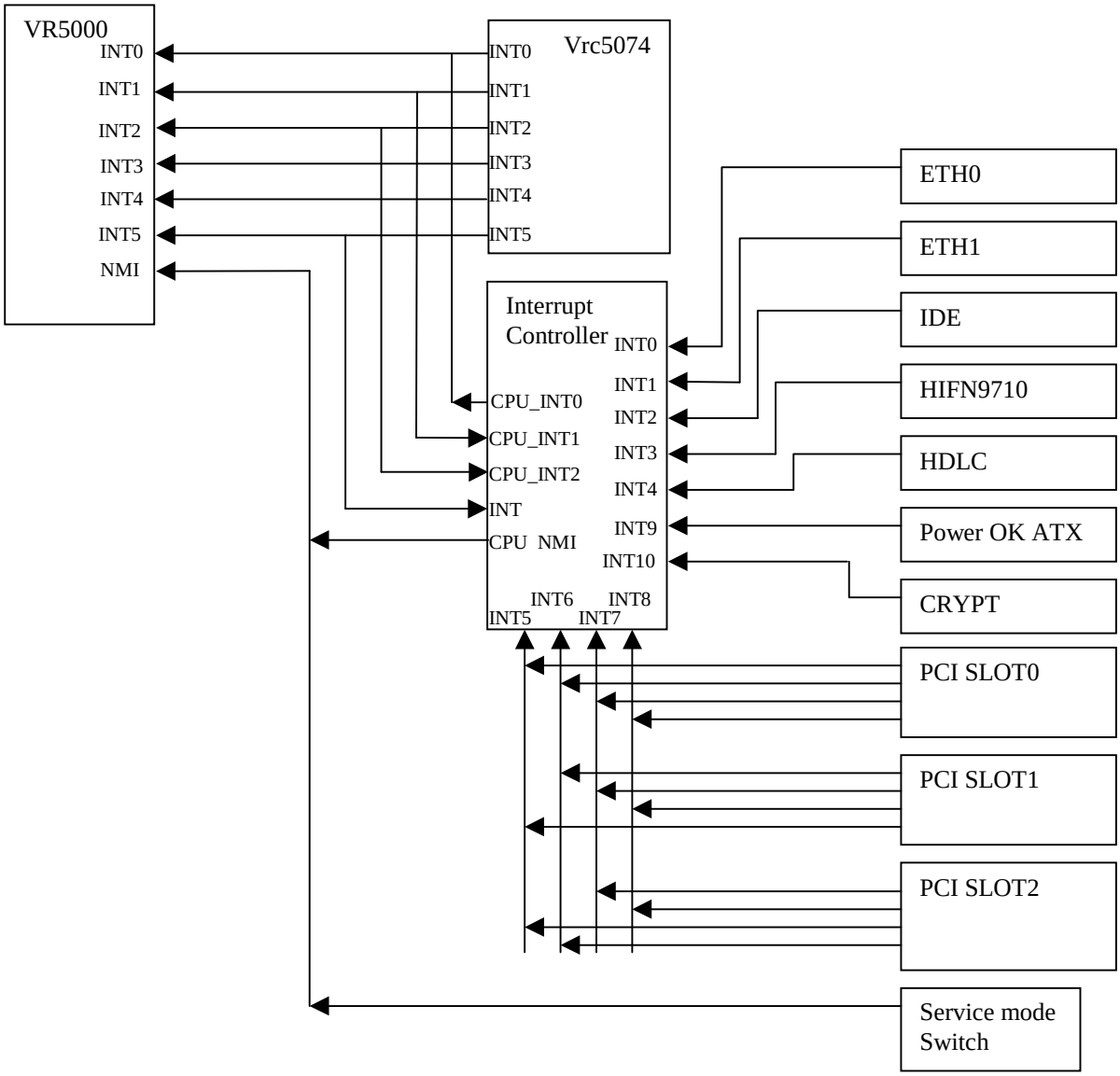
If both banks is used the System Controller has the possibilities for interleaved mode.

4.2.6 SECONDARY CACHE

The R5000 processor contains a dedicated secondary cache interface. These signals provide an efficient interface between the processor, the secondary cache, and the secondary cache tag RAM. All tag RAM interface signals (such as data and chip enables, output enable, address match, cache valid, line index, and word index) are provided by the R5000 processor. The secondary cache supports multiple cache sizes and both the write-through and write-back data transfer protocols. Data transfers to the secondary cache share the 64-bit system bus. The secondary cache can be configured as 512kB, 1Mbyte, or 2Mbyte. 1MByte are selected caused by second source. [9]

4.2.7 INTERRUPT

The VR5000 have support for 6 external interrupt sources and 1 NMI. The internal mask register for the interrupt lines aren't suitable for the Linux kernel. Therefor only one interrupt line is used (INT5) connected to an external interrupt controller. The Interrupt Controller is implemented in a FPGA, which has the user interface on the local bus. The interrupts are organized as followed:



Details for the Interrupt Controller is in the IntCtr_EAF Device document [11].

4.2.8 COMPRESSION

The compression processor chosen is HIFN9710. History memory minimum configuration is 1Mbyte/60ns EDO dram, supporting 64 histories. Each full-duplex compression/decompression history requires 16K bytes of ram storage, in LZS mode and 32K bytes in MPPC mode. Maximum dram memory size supported for this device is 32M bytes corresponding to 2048 LZS history buffers. DMA handshake interface can invoke the System Controller DMA channels.

If this is the case, the DMA gains control of the Local Bus and move the requested amount of data to a programmed memory location (SDRAM).

This device has register and memory interface for compression processor setup/status respectively history memory access. Reading/writing to the history RAM is enabled through a command stack register interface, see ref[7] page 12. Issuing a RAM read command includes setting a HISTORY # field , a SOURCE COUNT field and a DEST COUNT field. RAM address bits 24-14 are set by the entire HISTORY # field and RAM address bits 13-1 are set by bits 13-1 of the SOURCE COUNT field. The DEST COUNT field determines the number of bytes to read. When this command is issued, data can continuously (SOURCE COUNT value is incremented for each data read) be read in the DATA REGISTER, see ref[7] page 11. The history RAM interface supports only one command at a time, i.e. if a compression command has been started it must be terminated before a new command is given. This goes for RAM read/write commands as well. See ref[7] for full description.

Main board registers holds device reset, interface mode select and status on terminal count for source and destination dma transfers. By default this module is reset. To enable it, the appropriate interface mode must be programmed followed by a reset release (inactive). The mode supported in the first version is 01. Terminal count registers is only for hw measuring as the status is available in one dma cycle only and no latching capability is available in this register. See section.

4.2.9 RS232

Supports debugging in the prototype phase. It will not be mounted in the final version of the product. The circuit implements a minimum RS232 interface, including transceivers and connector. Data control is given through the System Controller UART. Maximum bit rate is 120K baud. Fail-safe circuit is included.

4.2.10 REGISTERS

Mapped as memory and includes the following functions:

- LCD display register interface (8 data and 3 control)
- Address filter/DMA registers
- RTC communication interface: RESET, DATA, CLOCK
- Boot map status
- Board ID eeprom: WRITE CONTROL, CLOCK, DATA
- Debug jumper status/test trigger output register
- Flash BUSY status
- Flash programming control
- Registered interface for the FPGA SRAM
- FLASH module present
- Control of LAN if crossing

See memory map section for detailed register definitions.

4.2.11 ID PROM

Is a 128 or 256 x 8 bit EEPROM accessible through the register interface, see previous description on SDRAM. It is intended for MAC addresses, box serial number, and other box configuration data.

4.2.12 RTC

Real Time Clock device. Generates elapsed time count. This must be converted to actual time by software. Access to this device is given through the register interface.
The RTC has an internal backup battery.

Chip: Dallas DS1603

4.2.13 HDLC CONRTOLLER

The HDLC-controller controls an external WAN link (V.35 or X.21). Addressing scheme is shown in section 4.

Requests:
- Minimum 64 byte FIFO.
- Support for DMA and interrupt.
- Minimum 2.66Mbit/s
- One channel.
- No CPU core.
- 16bit data interface, for the local CPU bus.

Chip: Siemens SAB82532-N-10 (16bit interface, dual, DMA mode)

4.2.14 TRANSCEIVERS

The transceivers are the physical interface to an external WAN link has 2 modes: V.35 and X.21.
Requests:
- Protocols: V.35 and X.21
- One connector for the 2 protocols.
- The connector type: DB25 or HDB44
- Hardware selectable protocol. Maybe cable selected with status register.
- 3 LED's in the front panel controlled by the firmware:
  Receive activity "Rx"
  Transmit activity "Tx"
  Link OK "Link"
- Loopback sceeme

Chip: Sipex SPS505

4.2.15 PCI ARBITER

The System Controller has arbitration for other 5 PCI devices and the Mother Board needs 6. Therefor an external arbitration is implemented. The System Controller supports both internal and external arbitration.

The external PCI arbiter will arbitrate for the PCI bus control on request from any master on the bus. When arbitration is done, it leaves control to the requesting part. Whenever 2 or more request bus control at the same time, a round robin arbitration scheme is applied. This means that if a master gets bus control it will be given lowest priority in a following arbitration, i.e. the priority will shift on each arbitration. This circuit will comply with PCI Specification rev 2.1.

An external arbiter will be implemented in a PLD.

4.2.16 IDE CONTROLLER

The IDE Controller is for the internal Harddisk.

Requests:
- Support for Ultra ATA 66MB/s.
- It will support standard disk drivers.
- Standard 40pin connector.
- Only one Disk drive connected. (Optional a slave-disk if no cost added to the mechanic).

Chip: CMD PCI0648 (Support for Ultra ATA66MHz)

4.2.17 ETHERNET CONTROLLER

Includes a 10/100 MAC controller with address filtering capabilities. A standard PCI interface and a DMA controller support data accesses without CPU intervention. Further issues like auto sense, promiscuous mode and LED control is available. The led control supports one Activity LED and one Link LED per controller. A MII interface sets signaling form to the LINE I/F.

Requests:

- MII interface for the address filter.
- Promiscuous mode allowing reception of all frames
- Signal switch on Tx and Rx for the RJ45.

Chip: AMD 79C972

4.2.18 ADDRESS FILTER

The Address Filter [10] can operate in either positive mode or in negative mode. In both modes the Ethernet Controller operates in promiscuous mode allowing reception of all frames. However, in negative mode the Address Filter will discard the frame if the Destination Address Field in the received frame matches with one of the Destination Addresses stored in the Address Filter. In positive mode the Address Filter will discard the frame if the Destination Address Field in the received frame do not match with one of the Destination Addresses stored in the Address Filter. In short positive mode allows reception of frames with an address match and negative mode allows reception of frames with no match.

The Address Filter can hold up to 4096 MAC addresses. These addresses are maintained by software through a set of commands. These commands are:

- InsertAddress.
- RemoveAddress.
- RemoveAll.

Each frame is decoded by analyzing nibbles on the MII interface. In this way the current MAC address is detected from the dataflow, and a search in the address filter is initiated. At the same time a busy status is indicated on the register interface. If a “hit” is detected it will discard the frame by signaling “invalid” to the Ethernet controller. This functionality is embedded in the Ethernet controller.

The Address filter, the DMA Controller and the interrupt controller are sharing the same FPGA device, Xilinx Spartan II 50K. The FPGA code is loaded through a registered connection to the local bus and the FPGA code it self is stored in the firmware FLASH.

4.2.19 DMA CONTROLLER ON THE LOCAL BUS

The System Controller has only 2 DMA channels. They are reserved for PCI and memory to memory access. The En/de-cryption, HDLC and the Compression chip need 3*2 DMA channels. The 6 DMA channels are integrated in a Xilinx FPGA. It has a 32 bit user interface on the local bus. The DMA Controller the Address-filter and the interrupt controller are sharing the same FPGA device. The FPGA code is loaded through a registered connection to the local bus and the FPGA code it self is stored in the firmware FLASH.

4.2.20 EN/DECRYPTION & HASHING COMPONENT (EDHC)

The Mother Board is prepared for hardware data en/decryption in a Virtec FPGA. It’s only an option if the VPN/NIC Board isn’t used.

Includes:

- DES and triple-DES encryption and decryption processor w/CBC.
- MD5 hash processor.
- Padding.
- Support for MD5-HMAC.

The interface to the LOCAL BUS implements:

- 32 bit data path.
- 9-bit address for internal register file.
- Reset control.
- Interrupt signaling.
- DMA handshakes.

Inside this device:

- Register file based command interface.
- 2Kbyte of dual-port RAM for data buffering before data processing.
- 2Kbyte of dual-port RAM for data buffering after processing.
- DES and triple DES processor.
- Registers holding three keys.
- Register for control of CBC mode.
- Register for control of data type (cipher-, plain-text).
- CBC IV register.
- Padding insertion/extraction.
- MD5 processor.
- Register for control of MD5 process (on/off).
- Offset register for buffer start to DES processing start.

The order of actions to be taken for a data buffer to be processed will then be as follows:

1. Copy data to EDHC processor.
2. Await interrupt.
3. Copy data from EDHC processor

4.2.21 Random Generator

The random generator is for the key to the data encryption. The random generator is based on diode noise, which is a true random source. The signal is amplified ,digitized and latch in to one bit on the board registers. The bandwidth off the random bit is 100Hz to 10MHz.

4.2.22 MISC CIRCUITS

Includes the following circuits:

- 2 X 16 character LCD display; (Firmware controlled contrast by EEPOTMETER or NTC).
- LCD backlight power
- Interface for 7 LED’s in the front panel
- Fan power
- Board power connection
- Hard disc power
- PSU
- Initial boot prom interface
- Reset circuit
- Test
- 2.5V/1A DC/DC
- 1.8V/3A DC/DC
- PCI Backplane

4.2.22.1 PCI_BACKPLANE

The Motherboard has a connector for a passive PCI Backplane. The Backplane includes 3 PCI slots. The Mother Board has provision for both 3.3V and 5.0V PCI Backplane.
It shall be possible to replace the backplane with a 90° PCI connector for single PCI board support.

4.2.22.2 VPN

HW encryption/decryption is achieved by mounting a PCI board with 2 Ethernet controllers and address filter on-board. Hardware support for IpSec.
The Motherboard is prepared for HW HW encryption/decryption from the SafePipe 100.

4.2.22.3 EXTERNAL HARDDISC EXPANSION

This is accomplished by using one of the three PCI slots for a FireWire or a SCSI adapter.

4.2.22.4 PSU

Power estimate:

Motherboard	25W
Harddisk	7W
PCI (3 slots)	30W (max 3*25W)
Total	62W

Each PCI slot (PCI Local Bus Specification 2.1):

5V ±5%	5A max. (System dependent)
3.3±0.3V	7.6A max. (System dependent)
12V±5%	500mA max.
-12V±10%	100mA max.

Specifications:

- Minimum 65W PSU giving 85-250V power connection
- 3.0–3.3V @ min. 10A
- 5.0–5.1V @ min. 5A
- 11.5-12.5V @ 2A
- -12V @0.5A
- (Net filter, main switch, fuse and Fan included)
- MTBF >100,000 hours
- ATX Connector

4.2.22.5 Fan

Possibility for an external Fan if there is no Fan in the Power Supply.
Specifications:

- DC Brushless
- Max size : TBD
- Operating Voltage: either 5V or 12V
- MTBF < 44000 hours (tacho. or temp feedback required)
- Fan on/off Control.

4.2.22.6 RESET CIRCUIT

Reset of all circuits is performed by a power monitor, and can be initiated by one of the following events:

- Whenever 1.8V or 3.3V or 5V powers up, or during operation if the voltage level falls below minimum.
- Reset button => hardware reset.
- Service button => NMI
- Reset register for overall system reset (SW control/warm reset).
- Finally in system PLD programming enabled, will also activate reset.

Reset of the processor is performed in 2 different levels: Cold Reset and Warm Reset.

The Cold Reset causes the processor to be totally reinitialized. Termination of the cold reset phase indicates that the 3,3V and 5 V DC power and the Master Clock to have been stable for more than 100 ms. At this time the processor

latches some basic configuration parameters (core clock multiplier, endian, output driver strength and boot device width).

The Warm Reset preserves the processor internal states. Causing internal processor state machines to be reset but preserves the contents in a number of internal registers. This feature enables some tracing to be performed, as a unique soft reset exception is executed after the warm reset. Furthermore SR bit in the processor status register will reflect this exception.

For the Processor below reset scheme is implemented:

Reset Source	Reset action
Power up or voltage drop	Cold Reset
Pld programming	Cold Reset
SYS Button	Warm Reset

All reset sources will give full reset of any PCI device, local bus peripheral, except for the reset source status flag registers, only reset by Cold Reset.

4.2.22.7 TEST

The PCB is prepared for ICT test. JTAG is not supported (The System Controller and the CPU does not support JTAG).

To support a provincial COM interface on the product even when the COM I/F is not mounted, a set of test points is given. They reveal the digital interface of the COM port, i.e. is the actual output signals of the system controller. In production test, the board specific test fixture must be able to connect to this interface and emulate a UART.

Test connectors provide easy logic analyzers measuring. The connectors used are AMP Mictor 38 pin headers - HP Logic Analyzer types pin-layout. Signals found in the connectors are primarily CPU/System Controller signals for initial HW debug.

4.3 Memory map

The memory map base addresses are fully programmable by software in the PDAR registers (Physical Device Address Registers). Base addresses must be set to define in which memory area the following device select signals are activated. Each of the device select signals will then enable resources/peripherals as shown in the table below. The Mother Board is used in 3 different configurations with 3 different memory maps.

Masquerade Pro				
Select line	Device	Physical Address	Size	Bus Width
SDRAM0	SDRAM Bank0	0.0000.0000- 0.07FF.FFFF	128MB	64
SDRAM1	-	-	-	-
DCS2 (UART_RTS)	FLASH Bank0/1 (boot FLASH connected)	0.1000.0000- 0.103F.FFFF	4MB	32
DCS3 (UART_CTS)	-			
DCS4 (UART_DCD)	HDLC	0.1200.0000- 0.121F.FFFF	2MB	16
DCS5 (UART_XIN)	Local Bus Registers (Address Filter, HDLC, Compression etc.)	0.1100.0000 0.111F.FFFF	2MB	32
DCS6 (DMA_ACK)	-			
DCS7 (DMA_REQ)	-			
DCS8 (DMA_EOT)	-			
PCIW0	PCI Address Window 0	0.1800.0000- 0.18FF.FFFF	16MB	32
PCIW1	PCI Address Window 1	0.1900.0000- 0.19FF.FFFF	16MB	32
INTCS	Internal Control Registers	0.1FA0.0000- 0.1FB0.0000	2MB	64
BOOTCS	i-data boot FLASH/ on board boot FLASH bank0	0.1FC0.0000- 0.1FFF.FFFF	4MB	32

Safepipe 200				
Select line	Device	Physical Address	Size	Bus Width
SDRAM0	SDRAM Bank0	0.0000.0000- 0.01FF.FFFF	32MB	64
SDRAM1	SDRAM Bank1	0.0200.0000- 0.03FF.FFFF	32MB	64
DCS2 (UART_RTS)	FLASH Bank0/1 (boot FLASH connected)	0.1000.0000- 0.10FF.FFFF	16MB	32
DCS3 (UART_CTS)	-			
DCS4 (UART_DCD)	HDLC	0.1200.0000- 0.121F.FFFF	2MB	16
DCS5 (UART_XIN)	Local Bus Registers (Address Filter, HDLC, Compression etc.)	0.1100.0000 0.111F.FFFF	2MB	32
DCS6 (DMA_ACK)	-			
DCS7 (DMA_REQ)	-			
DCS8 (DMA_EOT)	-			
PCIW0	PCI Address Window 0	0.1800.0000- 0.18FF.FFFF	16MB	32

PCIW1	PCI Address Window 1	0.1900.0000- 0.19FF.FFFF	16MB	32
INTCS	Internal Control Registers	0.1FA0.0000- 0.1FB0.0000	2MB	64
BOOTCS	i-data boot FLASH/ on board boot FLASH bank0	0.1FC0.0000- 0.1FFF.FFFF	4MB	32

Maximal Configuration				
Select line	Device	Physical Address	Size	Bus Width
SDRAM0	SDRAM Bank0	0.0000.0000- 0.07FF.FFFF	128MB	64
SDRAM1	SDRAM Bank1	0.0800.0000- 0.0FFF.FFFF	128MB	64
DCS2 (UART_RTS)	FLASH Bank0/1 (boot FLASH connected)	0.1000.0000- 0.11FF.FFFF	32MB	32
DCS3 (UART_CTS)	-			
DCS4 (UART_DCD)	HDLC	0.1200.0000- 0.121F.FFFF	2MB	16
DCS5 (UART_XIN)	Local Bus Registers (Address Filter, HDLC, Compression etc.)	0.1100.0000 0.111F.FFFF	2MB	32
DCS6 (DMA_ACK)	-			
DCS7 (DMA_REQ)	-			
DCS8 (DMA_EOT)	-			
PCIW0	PCI Address Window 0	0.1800.0000- 0.18FF.FFFF	16MB	32
PCIW1	PCI Address Window 1	0.1900.0000- 0.19FF.FFFF	16MB	32
INTCS	Internal Control Registers	0.1FA0.0000- 0.1FB0.0000	2MB	64
BOOTCS	i-data boot FLASH/ on board boot FLASH bank0	0.1FC0.0000- 0.1FFF.FFFF	4MB	32

After the Serial Mode EEPROM initializes the System Controller and the CPU at reset, the PDAR's turn off all physical address space except the chip-selects for the controller's internal register space INTCS and the Boot ROM BOOTCS.

Internal register control wait state generation. For programming guidance on VRC5074 internal registers see ref[2].

4.3.1 Boot map configuration

A reset exception will always use the vector address 1FC0.0000H. The System controller will then map this to BOOTCS and put the address 1FC0.0000H on the address bus. BOOTCS selects either boot sector in flash or "Initial Boot socket" inserted module as described previously.

4.3.2 PCI configuration map

For PCI configuration cycles following memory setup must be used:

Device	Configuration address
VRC5074, System controller	40.0000
PCI0648, Hard Disk controller	20.0000
Am79c972, Ethernet 10/100 controller "IN"	10.0000

Am79c972, Ethernet 10/100 controller "OUT"	8.0000
Expansion Module 2	4.0000
Expansion Module 1	2.0000
Expansion Module 0	1.0000

The above map is given by connecting the msb address lines on the PCI bus to the IDSEL line on each of the PCI devices.

4.3.3 UART Registers

The UART is included in the System controller, register memory space. See system controller datasheets for register specifications.

4.3.4 EEPROM addressing

See register 0 and register 4.

4.3.5 Local Bus Registers

Will take up 2 MByte address space for individual registers placed on 64K boundaries. The base address is defined by CS5 memory setup. All registers are 16 or 32bit. Within each 64K address sector, any register are then mirrored for each four bytes. Below is the address map with relative addresses

Rel. Address	Name Read/write	Description Read/Write
00000H – 0FFFFH	Register 0	EEPROM, RTC, FLASH status. Device resets, LAN X, FPGA prg. LCD display interface, LEDs. LCD display data
10000H – 1FFFFH	Register 4	PCI board present. FPGA prg status, FLASH/Backplane modulepresent. X.21/V.35 status, CPLD status.
2 0000H – 2 FFFFH	HDLC Controller	Device: SAB82532
3 0000H – 3 FFFFH	Compression	Device: HiFn9710
4 0000H – 4 FFFFH	Address filter/DMA	Device: FPGA Xilinx Spartan XCS30/XL
5 0000H – 5 FFFFH	Address filter/DMA	FPGA programming
6 0000H – 6 FFFFH	Crypt.	FPGA
7 0000H – 7 FFFFH	Crypt.	FPGA programming
8 0000H – 8 FFFFH	Soft Reset	Write only. When written a system reset (= cold boot) is generated.
9 0000H – 9 FFFFH		
A 0000H – F FFFFH		

Each of the above registers will now be defined in details.

4.3.5.1 Register 0 byte 0

Bit	Signal	Description
0	EEPROM_CS	EEPROM chip select, active low. (See datasheet 93C46)
1	EEPROM_CLK	EEPROM clock
2	EEPROM_DI	EEPROM data write
3	TIME_RST	RTC (Real Time Clock) reset. (See datasheet DS1603)
4	TIME_CLK	RTC clock.
5	TIME_DI	RTC data write.
6	FL_PRG	Flash program enable. "1" enables programming.
7	NOT_USED	Register, do not control anything.
Boot value		0000 0000x0

Init value	0000 0001x0
Data direction	Write (read back)

4.3.5.2 Register 0 byte1

Bit	Signal	Description
0	LAN1_X	Configures the LAN connector for port respectively station connections. Swap the receive and transmit signal pairs. 0: connections as in station mode 1: connections as in port mode
1	LAN2_X	Configures the LAN connector for port respectively station connections. Swap the receive and transmit signal pairs. 0: connections as in station mode 1: connections as in port mode
2	_COMP_RST	Compression reset, active low.
3	_ADDRF_RST	Address filter /DMA reset, active low.
4	_HDLC_RST	HDLC Controller reset, active low.
5	CPLD4	Not used.
6	ADDR_PRG_INITO	FPGA program signal, see the Xilinx Spartan datasheet. Signal inverted in hardware.
7	_ADDR_PRG_PRG	FPGA program signal, see the Xilinx Spartan datasheet.
Boot value		0000 0000x0
Init value		0001 1100x0
Data direction		Write (read back)

4.3.5.3 Register 0 byte2

Bit	Signal	Description
0	LCD_EN	Character Display Enable. Enables the character display for access. 0: Access disabled. 1: Access enabled.
1	LCD_RW	Character Display Read/Write. Defines the direction of data to or from the display. 0: Write (data to be stored in display) 1: Read.
2	LCD_RS	Character Display Register Select. 0: Command/Status 1: Data
3	LED0	LED0 Front panel, active high. ACT(ivity) on front panel for WAN
4	LED1	LED1 Front panel, active high. CON(nected) on front panel for WAN
5	LED2	LED2 Front panel, active high. Link on front panel for WAN
6	LED3	LED3 pcb debug.
7	LED4	LED4 pcb debug.
Boot value		0000 0000x0
Init value		0000 0000x0
Data direction		Write (read back)

4.3.5.4 Register 0 byte 3

Bit	Signal	Description
0	LCD_DB0	Holds the data to or from the character display
1	LCD_DB1	
2	LCD_DB2	
3	LCD_DB3	
4	LCD_DB4	

5	LCD_DB5	
6	LCD_DB6	
7	LCD_DB7	
Boot value		0000 0000x0
Init value		0000 0000x0
Data direction		Write (read back)

Tri-stated by LCD_RW(register 2). 0 = active, 1 = tri-stated

4.3.5.5 Register 4 byte 0

Bit	Signal	Description
0	_CRYPT_PRG_PRG	FPGA programming
1	_CRYPT_PRG_WR	FPGA programming
2	_CRYPT_RST	FPGA reset
3	CPLD6	Not used
4	CPLD0	CPLD code version bit 0
5	CPLD1	CPLD code version bit 1
6	CPLD2	CPLD code version bit 2
7	CPLD3	CPLD code version bit 3
Data direction		Bit0-3: Write(readback), Bit4-7: Read

4.3.5.6 Register 4 byte 1

Bit	Signal	Description
0	EEPROM_DO	EEPROM data read
1	TIME_DO	RTC data read
2	_PRSNT10	PCI Slot0
3	_PRSNT20	PCI Slot0
4	_PRSNT11	PCI Slot1
5	_PRSNT21	PCI Slot1
6	_PRSNT12	PCI Slot2
7	_PRSNT22	PCI Slot2
Data direction		Read

4.3.5.7 Register 4 byte 2

Bit	Signal	Description
0	FLM_PRSNT	Boot FLASH present, active high.
1	BP_PRSNT	PCI BackPlane present, active low.
2	No Connection	
3	NOISE	Random signal.
4	ADDR_PRG_INITI	FPGA program status. See Xilinx Spartan prg. Guide
5	ADDR_PRG_DONE	FPGA program status. See Xilinx Spartan prg. Guide
6	ADDR_PRG_DOUT	FPGA program status. See Xilinx Spartan prg. Guide
7	ADDR_PRG_LDC	FPGA program status. See Xilinx Spartan prg. Guide
Data direction		Read

4.3.5.8 Register 4 byte 3

Bit	Signal	Description
0	DTE_DCE_SEL	WAN DTE/DCE 0: DTE 1: DCE
1	V35_X21_SEL	WAN Protocol 0: X.21 1: V.35
2	_LOOPBACK	WAN test mode, active low
3	_CABLE_PRE	WAN cable present, active low
4		Not used
5	CRYPT_PRG_DONE	FPGA, programming status
6	_CRYPT_PRG_BUSY	FPGA, programming status
7	_CRYPT_PRG_INIT	FPGA, programming status
Data direction		Read

4.3.5.9 ADDRESS FILTER / DMA

See [10] [11]

4.3.5.10 Compression

See datasheet HIFN9710

4.3.5.11 HDLC Controller

See datasheet SAB82532

4.3.5.12 Soft Reset

Default value = not applicable.
Data direction = Write only

When written, this register activates the System Reset signal. This signal is also activated at cold boot. The value written to this register is “don’t care”

4.4 Connector Definitions

4.4.1 Initial boot, Flash Module

Has a 72 pin SIMM connector with the following pinout.

Signal Name	Connector Pin No.	Signal Name	Connector Pin No.	Signal Name	Connector Pin No.
GND	1	---	25	---	49
A10	2	D0	26	D25	50
A5	3	---	27	D29	51
A21	4	A7	28	D24	52
GND	5	---	29	D30	53
D2	6	VCC	30	D23	54
A3	7	---	31	D31	55

A19	8	A6	32	D22	56
D9	9	A14	33	D32	57
D19	10	A11	34	D21	58
D10	11	A8	35	D33	59
#RD	12	#CS	36	D20	60
D11	13	GND	37	D34	61
D7	14	A18	38	D18	62
D12	15	A12	39	#WR	63
D6	16	A17	40	A4	64
D13	17	A13	41	PRSNT	65
D4	18	A16	42	VCC	66
D14	19	---	43	GND	67
D4	20	A9	44	---	68
D15	21	D27	45	---	69
D3	22	A20	46	A15	70
D16	23	D28	47	GND	71
D1	24	A2	48	GND	72

VCC = 3.3V

4.4.2 Module Connection

Is given by a Metric angled PCI, complying to PCI Revision 2.1. Power keying is set for 5V.

Connector Pin No.	Signal Name	Connector Pin No.	Signal Name	Connector Pin No.	Signal Name	Connector Pin No.	Signal Name
1A	#TRST	1B	-12V	32A	AD16	32B	AD17
2A	+12V	2B	TCK	33A	+3,3V	33B	#C/BE2
3A	TMS	3B	GND	34A	#FRAME	34B	GND
4A	TDI	4B	TDO	35A	GND	35B	#IRDY
5A	+5V	5B	+5V	36A	#TRDY	36B	+3,3V
6A	#INT	6B	+5V	37A	GND	37B	#DEVSEL
7A	--	7B	--	38A	#STOP	38B	GND
8A	+5V	8B	GND	39A	+3,3V	39B	#LOCK
9A	--	9B	S1	40A	GND	40B	#PERR
10A	+5V(I/O)	10B	GND	41A	S2	41B	+3,3V
11A	--	11B	--	42A	GND	42B	#SERR
12A	GND	12B	GND	43A	PAR	43B	+3,3V
13A	GND	13B	GND	44A	AD15	44B	#C/BE1
14A	--	14B	--	45A	+3,3V	45B	AD14
15A	#RST	15B	GND	46A	AD13	46B	GND
16A	+5V(I/O)	16B	CLK	47A	AD11	47B	AD12
17A	#GNT	17B	GND	48A	GND	48B	AD10
18A	GND	18B	#REQ	49A	AD09	49B	GND
19A	--	19B	+5V(I/O)	50A	CONN KEY	50B	CONN KEY
20A	AD30	20B	AD31	51A	CONN KEY	51B	CONN KEY
21A	+3,3V	21B	AD29	52A	#C/BE0	52B	AD08
22A	AD28	22B	GND	53A	+3,3V	53B	AD07
23A	AD26	23B	AD27	54A	AD06	54B	+3,3V
24A	GND	24B	AD25	55A	AD04	55B	AD05
25A	AD24	25B	+3,3V	56A	GND	56B	AD03
26A	IDSEL	26B	#C/BE3	57A	AD02	57B	GND

27A	+3,3V	27B	AD23	58A	AD00	58B	AD01
28A	AD22	28B	GND	59A	+5V(I/O)	59B	+5V(I/O)
29A	AD20	29B	AD21	60A	S3	60B	--
30A	GND	30B	AD19	61A	+5V	61B	+5V
31A	AD18	31B	+3,3V	62A	+5V	62B	+5V

Note: Minimum requirement for a module is 5V PCI interface and keying.

4.4.3 PSU Connection

The main power connector is an ATX connector, Molex 39-29-9202.

Signal Name	Connector	Signal Name	Connector
	Pin No.		Pin No.
3.3V	1	+3.3V	11
3.3V	2	-12V	12
COM	3	COM	13
5V	4	PS_ON#	14
COM	5	COM	15
5V	6	COM	16
COM	7	COM	17
PWR_OK	8	-5V	18
5VSB	9	5V	19
12V	10	5V	20

4.4.4 Fan Connection 5V

2 Pin connectors of molex type 22-23-2021 or equivalent is used. Se pin-out below.

Connector	Signal Name
Pin No.	
1	5V
2	GND

4.4.5 Fan Connection 12V

2 Pin connectors of molex type 22-23-2021 or equivalent is used. Se pin-out below.

Connector	Signal Name
Pin No.	
1	12V
2	GND

4.4.6 Ethernet 10/100 UTP

Is an 8 pin RJ45 connector. See pin-out below.

Signal Name	Connector	Signal Name	Connector
	Pin No.		Pin No.
TX+	1	TX_CMB	5
TX-	2	RX-	6
RX+	3	RX_CMA	7

TX_CMA	4	RX_CMB	8

4.4.7 Debug port RS232

Is an 6 pin header. See pin-out below.

Signal Name	Connector Pin No.	Signal Name	Connector Pin No.
RXD_104	2,5		
TXD_103	1,6		
GND_102	3,4		

4.4.8 Lattice pld programming interface

Is an 8 pin sil connector of AMP type 640452-8 or equivalent. Pin no 4 in this connector is left blank, to ensure that no polarization error will occur when connecting to the cable part.

Signal Name	Connector Pin No.	Signal Name	Connector Pin No.
SCLK	1	#ISPEN	5
GND	2	SDI	6
MODE	3	SDO	7
--	BLANK	VCC(5.0V)	8

4.4.9 LCD

- 2 Pin connector of molex type 22-23-2021 or equivalent is used. Se pin-out below.
- 10 Pin connector for the datainterface.

Connector Pin No.	Signal Name
1	5V
2	GND

4.4.10 IDE Interface

- 2 connectors for the IDE Interface. 40pin dual in line connector.

Pin	Description	Pin	Description
1	Reset	2	GND
3	Data7	4	Data8
5	Data6	6	Data9
7	Data5	8	Data10
9	Data4	10	Data11
11	Data3	12	Data12
13	Data2	14	Data13
15	Data1	16	Data14

17	Data0	18	Data15
19	GND	20	Key
21	Reserved	22	GND
23	IOW	24	GND
25	IOR	26	GND
27	IO Chrdy	28	Ale
29	Reserved	30	GND
31	IRQ14	32	IOCS16
33	Addr 1	34	Reserved
35	Addr 0	36	Addr 2
37	CS0 (1F0 - 1F7)	38	CS1 (3F6 - 3F7)
39	Active	40	GND

4.5 Mechanical Description

4.5.1 Design Constraints

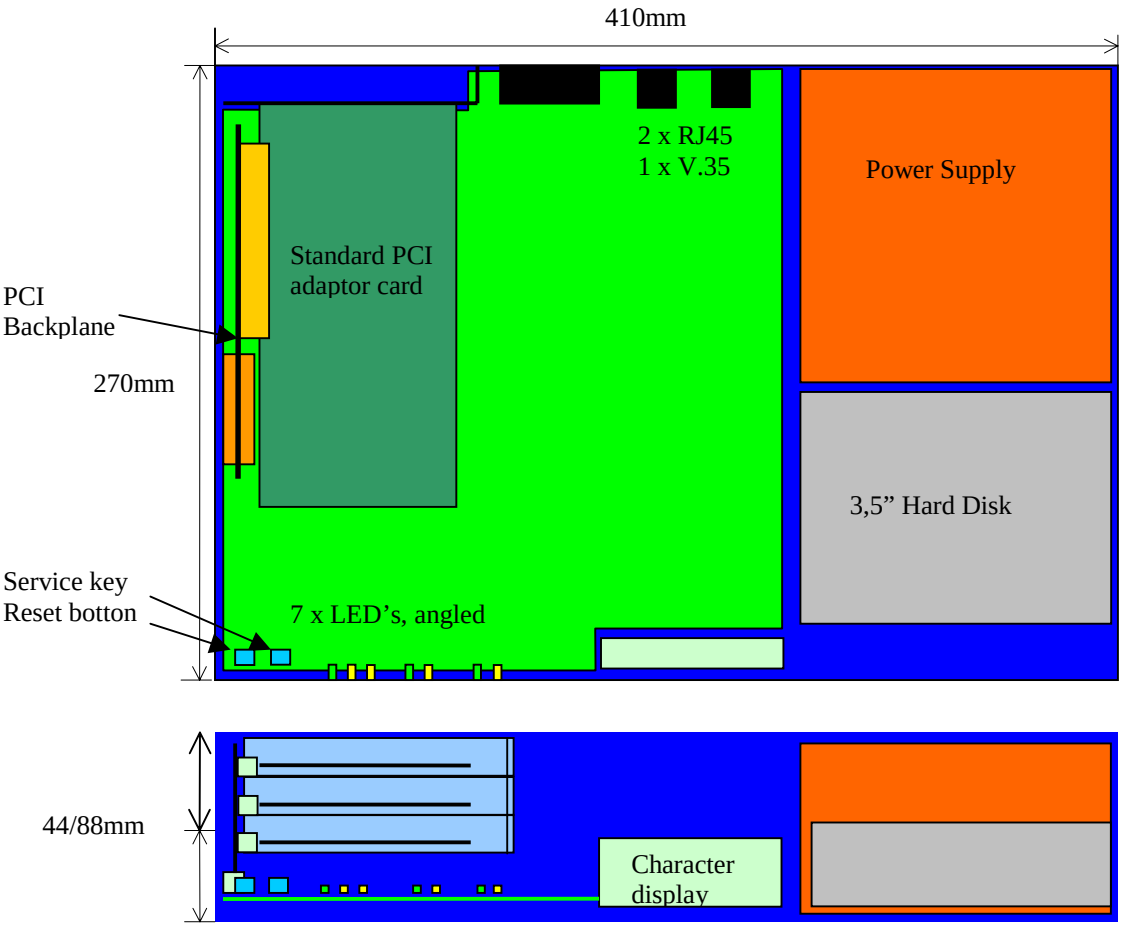
The design constraints for the VPN Pro BOX is given below:

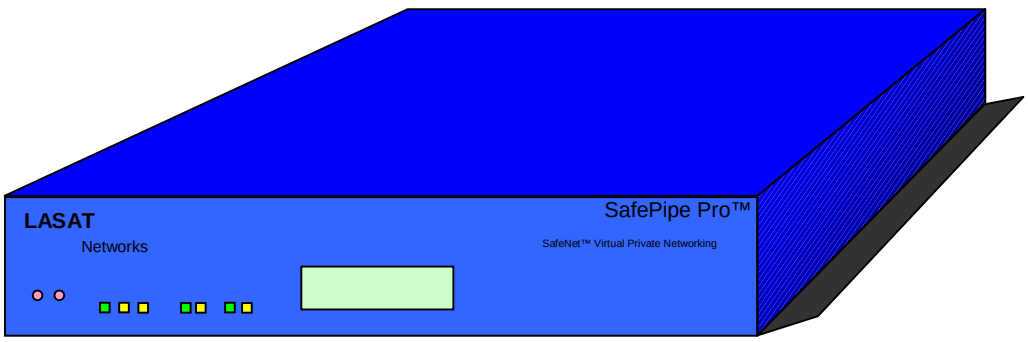
- The height of the box is 2U (88.9mm).
- Form factor for depth/length is 262mm/436mm
- Provision for 19" rack mounting.
- Esthetic design (i.e. an industrial designer is required).
- All cable attachment to the box is on the back
- Three PCI slots for a standard PCI-card.
- PCI devices vertical mounted.
- Front bracket of the PCI card is accessible from the rear of the box.
- 2 RJ45 connectors for LAN (WAN) connections on the rear.
- One V.35/X.21 connector for LAN/ WAN connections on the rear.
- 7 LED's on the front showing :

  Ethernet (Internet): "Link" and "Activity"
  Ethernet (Local Network): "Link" and "Activity"
  WAN (V.35/X.21) "Rx", "Tx" and "Link"
- "Link" LED's are green.
- "Activity", "Rx" and "Tx" LED's are yellow.
- Push button for system initialization. Accessible from the front through a hole in the front panel.
- Service button
- Character display (2 lines, each of 16 characters) on front.
- One 3,5" hard disc. (Optional slave-disk, no cost added).
- Fan for cooling.
- Power Supply
- EMC correct design.
- IEC Power Inlet with filter on the rear.
- Mains switch on the rear.

4.5.2 The Box

A drawing of the VPN Pro BOX is shown below. The drawing is not meant to a final design but rather a visualization of the various parameters, which have to be considered during the final design of the box.

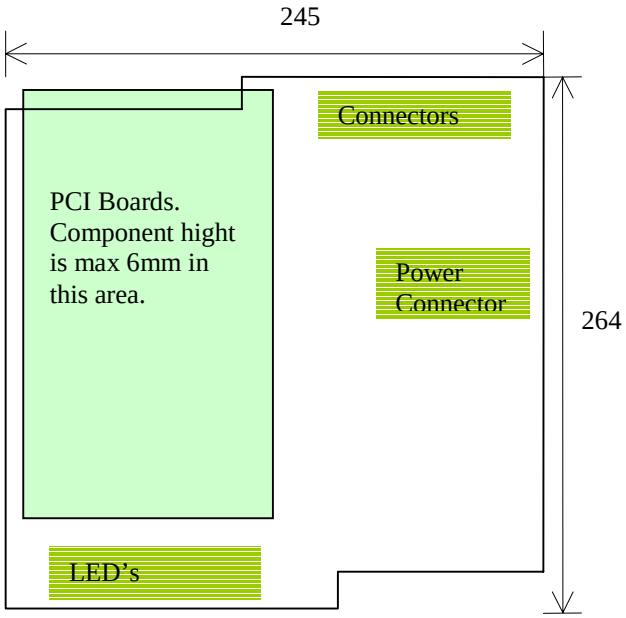




4.5.3 PCB Outline

The figure below shows the PCB outline. The PCB will be 10 layers of which 6 are dedicated to power distribution. Components are placed one side only.

The PCB must comply with i-data guidelines for PCB layout and manufacturing.



All dimensions in mm

Layes:
1. Components
2. Power
3. Signal 1
4. GND
5. Signal 2
6. Signal 3
7. GND
8. Signal 4
9. GND
10. Solder

4.6 Approvals and Compliance

4.6.1 V.35

Kim Boll

4.6.2 X.21

Kim Boll

4.6.3 EMC

Kim Boll

4.6.3.1 Electromagnetic Interference Performance

Electromagnetic Interference performance is tested with reference to the requirements shown below. The VPN Pro BOX, including all peripherals, must meet:

Region	Regulation, Shielded Cable	Regulation, Unshielded Cable
Europe	EN55022, Class B	EN55022, Class A
North America	FCC, part 15, subpart B Class B.	FCC, part 15, subpart B Class A.
Japan	VCCI class B	VCCI class A
Other	CISPR 22, Class B	CISPR 22, Class A

4.6.3.1.1 Power Line Harmonic Distortions

Comply to IEC 1000-3-2.

4.6.3.2 Electromagnetic Susceptibility Performance

Compliance to EN50082-1, incl. normative and informative annex, or EN55024.

4.6.4 Product Environment

4.6.4.1 Temperature and Humidity Environment

Product Power On:

Dry Bulb Temperature:	10 to 40 deg. C
Relative Humidity:	8 to 80 % non condensing
Wet Bulb Temperature:	27 deg. C

Product Power Off:

Dry Bulb Temperature:	10 to 52 deg. C
Relative Humidity:	8 to 80 % non condensing
Wet Bulb Temperature:	27 deg. C

Note :Assuming laminar air flow in area of card, the cooling capabilities of the chassis when in operating configuration shall not allow the air ambient box temperature to exceed 70 deg. C.

4.6.4.2 Altitude

0 to 3000 meters corresponding to the absolute pressure of 106 KPa down to 70 KPa.

4.6.4.3 Storage and Shipment Environment

Storage :

Dry Bulb Temperature :	1 to 60 deg. C
Relative Humidity :	5 to 80 %
Wet Bulb Temperature :	29 deg. C

Shipment :

Dry Bulb Temperature :	-40 to 60 deg. C
Relative Humidity :	5 to 100 %
Wet Bulb Temperature :	29 deg. C

4.6.4.4 Vibration and Shock Requirements

Shock & Vibration exposures are specified below related to the scenario:

- Simulated Product Transportation

4.6.4.4.1 Transportation

To simulate the product transportation environment, products shall undergo the tests described below. During exposure, the EM is inserted in the switch enclosure, and the enclosure is in retail packageing.

a) Random Vibration
The test is performed according to IEC 68-2-36, Test Fdb, Random Vibration, specified as follows:

Total rms acceleration	:	$1g_{rms}$
Acceleration Spectral Density (ASD) 10-20 Hz	:	$0.02g^2/Hz$
ASD 20-150 Hz	:	-3dB/octave
Duration pr. axis	:	30 min.

b) Bump
The test is performed according to IEC 68-2-29, Test Eb, Bump, specified as follows:

Bump amplitude	:	25g
Bump duration	:	6ms
Bump directions	:	3 mutually perpendicular
Bump repetitions	:	1000 pr. direction

c) Free fall
The test is performed according to IEC 68-2-32, Test Ed, Free Fall, specified as follows:

Height of Fall	:	0.6 to 1.2m
Number of falls	:	12, two in each attitude as given below
Test Surface	:	Concrete
Fall Sequencing	:	One fall on each side

4.6.5 Product Marking and Labelling

Product Marking consists of a Bar-code Label with serial number and product ID.
Product approvals and marking of:

- C-UL
- UL
- CE
- CE-according to tele terminal directive.
- FCC, part 15 & 68

4.6.6 Safety requirements

- IEC 950:Latest Edition - Safety of Information Technology Equipment, Including Electrical Business Equipment.
- UL 1950, Latest Edition.
- CSA Standard CAN/CSA-C22.2 No. 950 - Safety of Information Technology Equipment, Including Electrical Business Equipment
- EN 60950:Latest edition (CENELEC country deviations to IEC 950).

5. Test Specification

5.1 Design Verification Test

6 pieces of 20/80 pin connectors fitting a logic analyzer pots (ex. HP), are put on the PCB connecting to the basic cpu bus (control signals included). Further derived essential control signaling will also be supplied. Smallest possible

interaction to preferred PCB layout must be obtained in placing the 6 connectors. This interface will enable debugging of HW and SW implementations. The Molex type 5332/20 pin connector is suggested for this test interface.

5.2 Production Test

The PCB will have test points on almost every net which makes it possible to perform an In Circuit Test (ICT) of the board. Circuit design and PCB layout, must comply with ICT demands, i.e. issues like spacing, terminating free pins, etc. must be considered.

JTAG will optionally be supported.

5.3 Test Programs

During the Design Verification Test and Production Test various types of test programs will be needed. These test programs must have following functionality:

- Tbd

6. Cost estimate

The cost estimate is based on qty. 1000. It includes all functions.
In the SafePipe 200 configuration are the Ethernet, Address Filter and the IDE Controller removed. This reduce the prices by $50.44 + $11 + $21 = $81.44.

PCI Adapter Card for VPN functionality adds $240.

Function	Description	Qty.	Std.Price	Total	Sub.
CPU System	VR5000-200	1	60	60	
	VRC5074	1	39	39	
	DC/DC 1.8V 3.3V 3A	1	10	10	
	L2 Cache 512K (64k*18) MCM69P618	2	5	10	
	TAG SRAM MCM69T618	1	22	22	
	LATTICE ISPLSI2032 PLD (PCI ARBITOR)	1	2	2	
	FLASH 32Mbit (2M*16bit)	4	8.5	34	
	SDRAM MODULE 32Mbyte 168 PIN	2	35	70	
	CONNECTOR 168P DIMM (SDRAM)	2	2	4	
	REAL TIME CLOCK (RTC)	1	4.5	4.5	
	CONNECTOR 72P DIMM (INIT. BOOT SOCKET)	1	2	2	
	EEPROM 2K SERIAL 2-W SO8, AT24C02N-10	1	0.4	0.4	
	ISPLSI2032 (glue logic)	3	2.5	7.5	
	SWITCH PUSHBUTTON SPST	1	0.15	0.15	
	SUPPLY SUPERVISOR 4.63V MAX809 SOT23	1	0.35	0.35	
	SUPPLY SUPERVISOR 2.93V MAX809 SOT23	1	0.35	0.35	266.25
Ethernet:	AMD 79C792 PCI 10/100 ETH CNT.	2	13	26	
	BCM5201 PHY 100BTX/FX/10BT MII TQFP64	2	5.5	11	
	CRYSTAL 20MHz 20pF 20/F 50/T HC49S	2	0.5	1	
	OSCILLATOR 25MHz 100PPM 40/60	2	0.96	1.92	
	CONN. 8P. PHONE SHIELDED 8/8	2	0.28	0.56	
	TRANSFORMER 10/100B-TX F.ML6692 SMD16	2	1.7	3.4	
	FERRITE FILT WIDE 600R/100MHZ 200mA 0805	6	1	6	
	INDUCTOR 330nH 20% 1210	4	0.14	0.56	50.44
HDLC, V.35/X.21	SAB82532	1	10	10	
	LTC1344	1	10	10	
	LTC1343	1	5	5	
	D-SUB 25	1	1	1	26
IDE	PCI0648	1	10	10	
	40 pin connector	1	1	1	11
Address Filter:	SRAM 32K*8 20NS 3.3V	1	1	1	
	Xilinx Spartan 20K VQ100 –4	1	17	17	18
Glue Logik	Buffers	8	0.3	2.4	
	Clock Drivers	1	1	1	3.4
Display	LCD 2*16 char	1	10	10	
	LED	10	0.2	2	12
PCI Backplane	3 PCI slots +connector +PCB	1	20	20	20
Misc.	Res., Cap, Diodes, Trans, etc	300	0.02	6	6
PCB	300*400 8-layers	1	40	40	40
Harddisk	2GB	1	100	100	100
Mechanics:	BOX	1	30	30	
	Blind plate, PCI	3	0.8	2.4	
	FAN	0	5	0	
	PSU	1	30	30	
	POWER INLET W. FILTER	0	4	0	
	POWER SWITCH	0	3	0	
	Misc (Screws, Nuts, Gaskets, etc)	1	3	3	65.4
TOTAL:				618.49	618.49
Overhead:	20% of costprice			123.698	
GRAND TOTAL				742.188	

7. Future Enhancements

The below functionality will be considered for future product enhancements

- Tamper proof Enclosure
- Hardware protection off the software license