HARDWARE DESIGN SPECIFICATION

i-data international confidential

| in margin marks changes from revision 0.00

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1. Document log.

Date	Init.	Revision	Changes
981102	LCH	0.00	Template created.
981102	LCH	0.01	Issued for Document review.
981130	LCH	1.00	Comment from review included.
981221	LCH	1.01	Hard disc size changed from 2,5" to 3,5". Logo Definition added
991021	LCH	2.00	Changes to whole document reflecting actual implementation of hardware in PCB Rev. 218.2
991027	JAL	3.00	Substituting IDT processor system with NEC and Galileo are reflected in chapter 3, 4 and 5.
200106	JAL	3.01	UART and ISDN controller moved in memory map

2. General

This document specifies and defines the function of the VPN BOX.

The primary function of the VPN BOX is to provide a secure and private communication path over the Internet either between to LAN's or between a LAN and a Remote PC.

The main features of the VPN BOX includes:

- Access to two LANs (10/100Base-TX).
- Routing
- ISDN access
- Encryption
- Authentication
- Internet Key Exchange (IKE)
- PCI socket for 1 standard PCI Card

2.1 Document reference

[1] Am79C972 Datasheets rev B
Enhanced 10/100 Mbps PCI Ethernet Controller
[2] GT-64115 Datasheet rev1.0
Galileo Technology, MIPS-4000-Family System Controller Chip
[3] Vr4300, Vr4305, Vr4310 Datasheets, 5th edition
NEC R4000 core based 64 bit Processor
[4] PSF21525 Datasheets rev2.1
High Level Serial Communication Controller, 2 hdlc channels
[5] Fujitsu Flash Memory databook

[6] PCI Local Bus Specification
Revision 2.1, June 1, 1995.
[7] HiFn9710, Data Compression Coprocessor Data Sheets
Revision 1.2, September, 1997.
[8] Picvue Electronic LCD module databook.

[9] Vr4300, Vr4305, Vr4310, Hardware User's Manual
Embedded 64 bit Microprocessor
[10] PSB 21525, Hardware User Manual 02.96
High-Level Serial Communication Controller Extended
[11] PSB 2186, Hardware User Manual 10.94
ISDN Subscriber Access Controller for Terminals

2.2 Overview

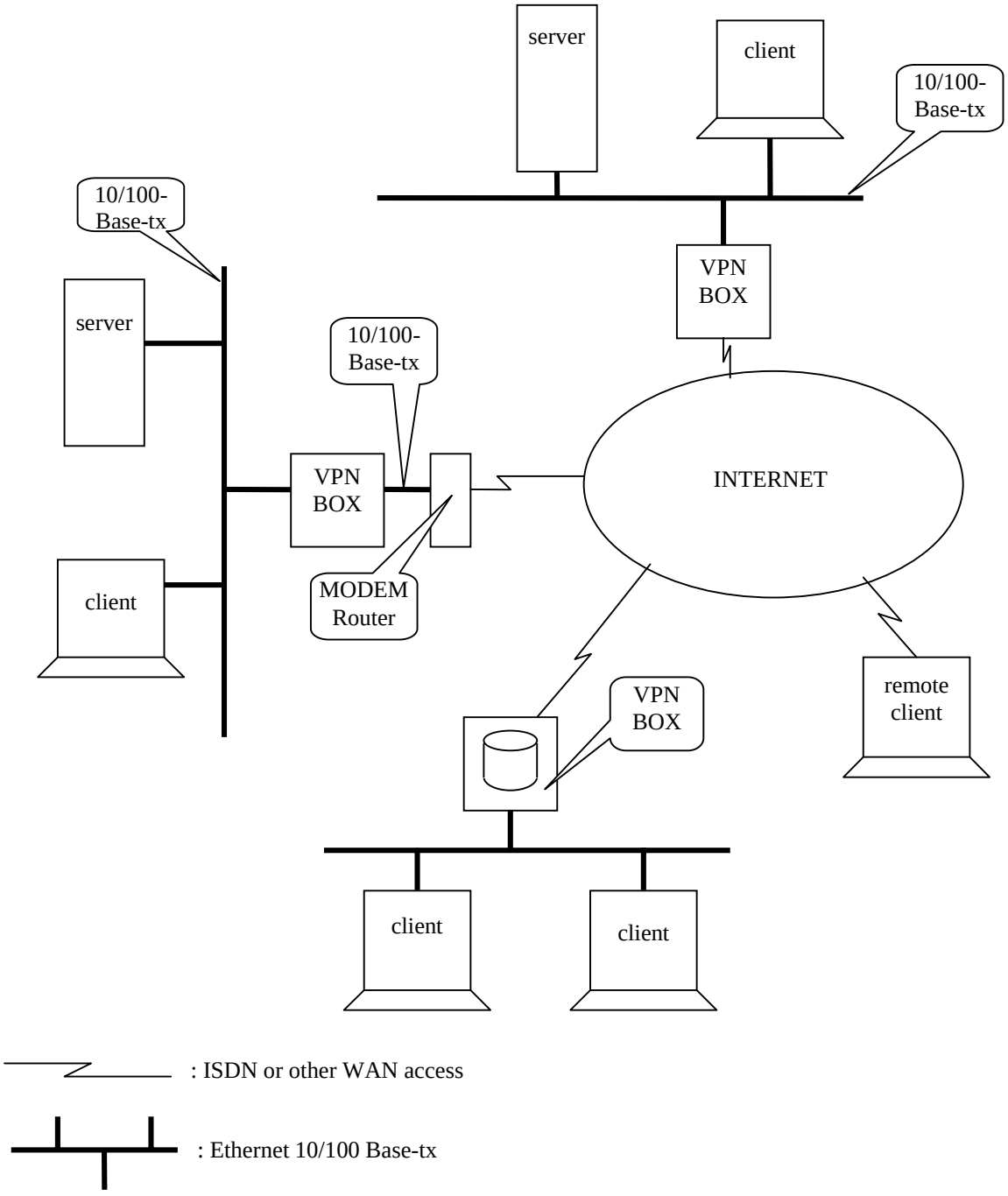
Project name:	<DCG Project name>		
Basis product:	<MOW Basis Product Name>	<S-number>	<Comp number>
Variants:	<MOW Basis Product Name>	<S-number>	<Comp number>

2.3 Abbreviations

IPSec	IP Secure
LAN	Local Area Network
VPN	Virtual Private Network
IKE	Internet Key Exchange
BRI	Basic Rate Interface

3. Product Description

The VPN BOX is a stand-alone unit intended to provide a secure communication path between two LANs or between a LAN and a Remote Client. The figure below shows the environment for the VPN BOX



The function of the VPN BOXes is:

- **Net-to-Net VPN**: Provides a secure IPSec tunnel to another VPN BOX across the Internet. Inside this tunnel a various number of protocols to can be transferred between networks. Some protocols are native (i.e. known an understood by the VPN BOX). These protocols can be efficiently routed between the networks (through the tunnel). Other protocols must be bridged. However this may require changes in the configuration of the devices attached to the network.

- **Remote Access VPN:** Provides a secure IPSec tunnel to a single user located somewhere on the Internet. The effect of this VPN BOX is to "short-circuit" this user through the tunnel to the internal network, so it looks like the user is attached to the LAN. This method uses a similar function to bridging for all protocols.

The VPN BOX will have following interfaces:

- An interface (with MAC Address filtering) to the internal 10/100 Mbps Ethernet.
- A 10/100 Mbps Ethernet interface towards Internet. This interface implies that an external Modem or similar is connected between the Ethernet and Internet.
- An ISDN basic rate interface providing direct connection to the Internet.

Three different VPN Boxes are defined:

1. A pure VPN with hardware filtering on the internal LAN interface and with software encryption/decryption or hardware accelerated encryption/decryption.

2. A small Masquerade with all the Masquerade software installed. This includes firewall, mail-server and web-server. This configuration requires an external file-server.

3. A large Masquerade with the same software as the small Masquerade but with a hard disc drive installed.

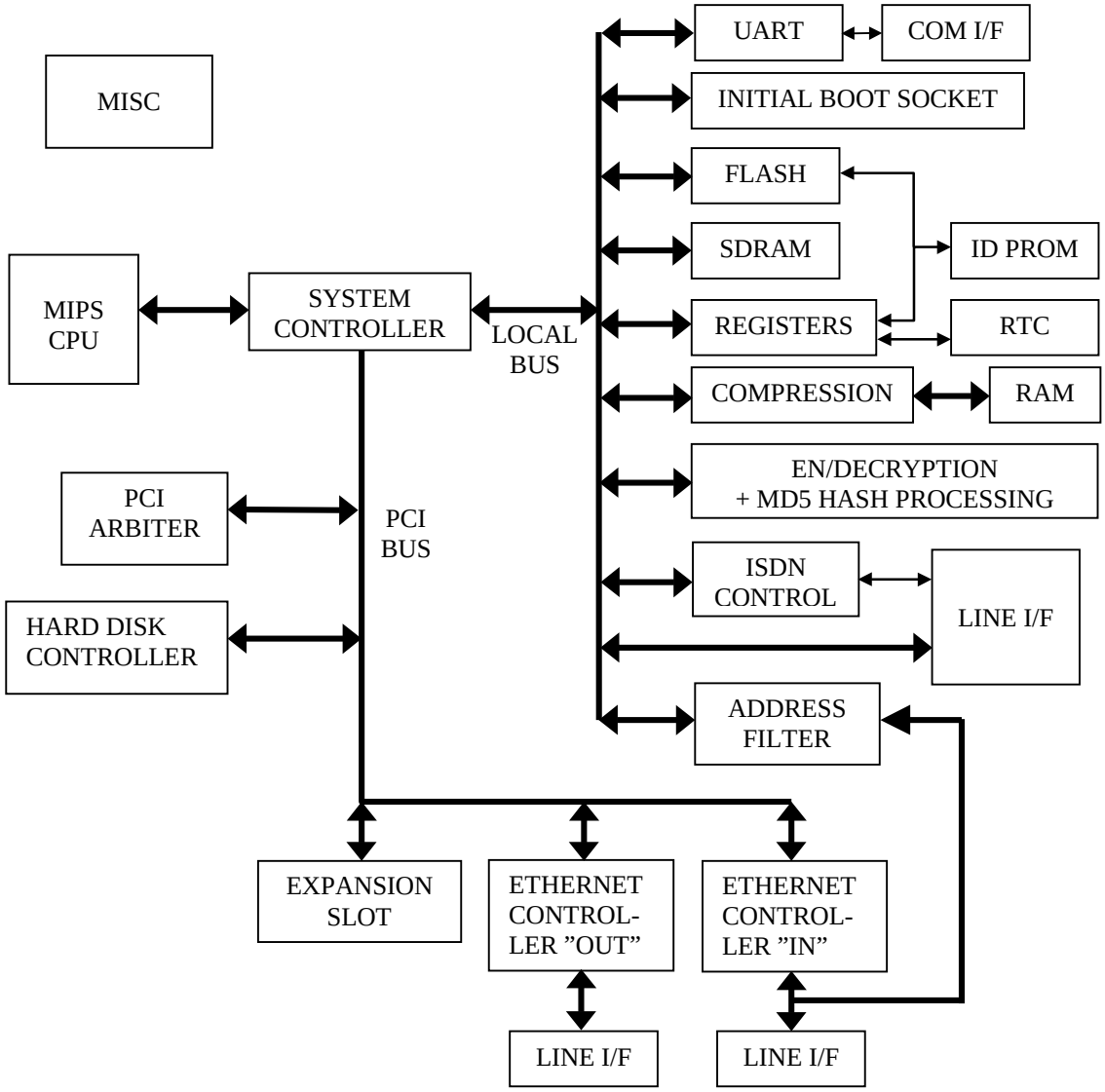
The table below defines the hardware for the 3 configurations:

	HW En/De-cryption	HW Compression	Address Filter	Hard Disk
1. Pure VPN	Yes	Yes	Yes	No
2. Small Masquerade	No	No	No	No
3. Large Masquerade	No	Yes	Yes	Yes

4. Hardware Description

Now the hardware design will be defined. The following subsections show the overall functional blocks and interconnections. Detailed descriptions of implementation and use are explained, and any interfaces are described.

4.1 System Block Diagram



The above figure shows the basic structures and functional blocks of the design. A system controller implements a LOCAL BUS for processor peripherals, and a PCI BUS for system peripherals.

4.2 Functional Description

Divided into subsections explaining the circuit blocks shown in the above System Block Diagram.

4.2.1 MIPS CPU

Is a 64-bit MIPS RISC processor with 32 bit bus interfaces. It operates at a frequency of 100MHz, 133MHz or 166MHz giving a max performance of 221 dhrystone MIPS. The NEC Vr4310 processor is selected, and has the following features:

- 16Kbytes instruction cache
- 8Kbytes data cache
- 2-way set associative cache
- Write-back write-through support on per page basis
- Scalar 5-stage pipeline
- 5 interrupt lines
- 32 bit multiplexed data and address bus
- Little endian
- Bus error exception

Interrupt sources as table below shows.

Interrupt source	CPU interrupt channel
Service Mode Push Button	NMI
Common interrupt (all board interrupt sources or'ed on this line)	INT0
Not used	INT1
Not used	INT2
Not used	INT3
Not used	INT4

All interrupt inputs on the processor are level sensitive only. The processor does not implement a hardware solution for prioritizing interrupts. Software must handle prioritizing by an enable/disable scheme in the interrupt mask register (see 4.3.5.8). Chapter 6 in the manual describes how exceptions (and interrupts) are handled in the CPU.

Accesses in address area not valid, i.e. not selecting any memory or devices will generate a "bus error" signal to the processor. This will initiate a bus error exception.

See ref[3] for detailed processor description.

4.2.2 SYSTEM CONTROLLER

Implements address/data bus demultiplexing, programmable wait state control, sdram controller, PCI interface, 4 Timers, 4 DMA controllers.

4.2.3 INITIAL BOOT SOCKET

Is a socket for a standard i-data flash module. Preprogramming such a module with boot code and possible some part of or all the application code, it can be inserted into the board and be used as boot memory. When a module is inserted it configures the boot circuit to boot from this memory whereas the onboard flash is mapped into another memory area. Flash module status "inserted" is then visible in the board registers. In this state the defined boot sector in on board flash will be enabled for programming. Flash on the module can not be programmed from the board.

4.2.4 FLASH

Is 1 M, 2M, 4M or 8 Mbytes of flash. Not upgradable from one size to another. The first Mbyte of flash is defined as boot area, and given special attention with regards to protection and visibility in the memory map. When the “initial boot socket” is empty the boot sector is mapped into the boot memory (BFC0.0000 and above). The boot memory is write protected and register status shows “no module inserted”.

To be able to support the full range of memory size configurations, the PCB layout has 2 device positions supporting 4Mbit, 8Mbit, 16Mbit or 32Mbit devices all in a tsop package. As they are footprint compatible it then implements 256K X 32bit, 512K X 32bit, 1M X 32bit or 2M X 32bit equal to 1M, 2M, 4M or 8M bytes of flash memory. The layout is also applicable for simultaneous read, write types of flash (in a tsop package). The preferred selection of flash devices is the AMD/Fujitsu boot sector inherent 3,3V flash devices. These come in 2 versions, one with the included boot sector placed in the beginning and one in the end of the flash. As this boot sector will not be used in this product as boot sector, we will chose the version with the inherent boot sector in the end of the flash address area.

When the “initial boot socket” has a module inserted, the module memory is mapped into the boot memory (maximum of 4Mbyte available). Detection of this will enable the on board flash boot sector for programming and in board registers show status of a module inserted.

Flash memory is also given a permanent memory location. This is SW programmable through registers in the System Controller, see 4.3. To be able to program any part of the flash, additional write protection (in board registers) must be disabled. This also goes for boot sector programming when a module is inserted.

4.2.5 SDRAM

A 168 pin standard sdram SIMM connector will support 16Mbytes to 128Mbytes of sdram. Module configuration data is accessible in an eeprom on the module. To access configuration data the EEPROM_COMM register must be used, see section 4.3.5.2. It includes a common eeprom communication interface, divided between the sdram module eeprom and the board id prom. Write protection of the sdram eeprom is fixed to “protected”. Addressing in the serial data stream to any of the eeprom’s does selection of either. Addressing scheme is shown in section 4.3.4.

4.2.6 UART

Is a standard 16550 type UART see datasheets on TL16550. No handshake signaling is implemented (only txd and rxd). Possible baud rate settings is given by the oscillator signal supplied to the UART. This frequency is selected to 73728MHz. The UART implements an interrupt source to the interrupt controller, see section 4.3.5.7.

4.2.7 COM I/F

Supports debugging in the prototype phase. It will not be mounted in the final version of the product. The circuit implements a minimum RS232 interface, including transceivers and connector. Data control is given through the preceding UART. A 6 pole pin header is used for cable connection. Maximum bit rate is 120K baud. Fail-safe circuit is included.

4.2.8 REGISTERS

Mapped as memory and includes the following functions:

- Control of ISDN I/F LED’s
- System button flag (for system initialization, during boot)
- LCD display register interface (8 data and 3 control)
- Address filter registers
- Dram module eeprom clock control bit
- Dram module eeprom data i/o bit
- RTC communication interface, RESET

- RTC communication interface, DATA
- RTC communication interface, CLOCK
- Boot map status
- Board ID eeprom, WRITE CONTROL
- Board ID eeprom, CLOCK
- Board ID eeprom, DATA
- Debug jumper status/test trigger output register
- Flash BUSY status
- Flash programming control
- Compression device reset
- Compression device interface select control
- Compression device terminal count status (destination & source)
- En/Decryption + MD5 Hash processing device reset control
- FPGA programming control and status
- Interrupt status and mask registers

See memory map section for detailed register definitions.

4.2.9 ID PROM

Is a 128 or 256 x 8-bit eeprom accessible through the register interface, see previous description on SDRAM. It is intended for MAC addresses, box serial number, and other box configuration data.

4.2.10 RTC

Real Time Clock device. Generates elapsed time count. This must be converted to actual time by SW. Access to this device is given through the register interface. See section 4.3.5.2.

4.2.11 COMPRESSION

The compression processor chosen is HIFN9710/9711. All these 4 devices need to be supported. History memory minimum configuration is 128Kbyte/12ns SRAM, supporting 8 histories. Each full-duplex compression/decompression history requires 16K bytes of ram storage, in LZS mode and 32K bytes in MPPC mode. DMA handshake interface can invoke the System Controller DMA channels. If this is the case, the DMA gains control of the Local Bus and move the requested amount of data to a programmed memory location (sdram).

This device has register and memory interface for compression processor setup/status respectively history memory access. Reading/writing to the history RAM is enabled through a command stack register interface, see ref[7] page 12. Issuing a RAM read command includes setting a HISTORY # field, a SOURCE COUNT field and a DEST COUNT field. RAM address bits 24-14 are set by the entire HISTORY # field and RAM address bits 13-1 are set by bits 13-1 of the SOURCE COUNT field. The DEST COUNT field determines the number of bytes to read. When this command is issued, data can continuously (SOURCE COUNT value is incremented for each data read) be read in the DATA REGISTER, see ref[7] page 11. The history RAM interface supports only one command at a time, i.e. if a compression command has been started it must be terminated before a new command is given. This goes for RAM read/write commands as well. See ref[7] for full description.

Main board registers holds device reset, interface mode select and status on terminal count for source and destination DMA transfers. By default this module is reset. To enable it, the appropriate interface mode must be programmed followed by a reset release (inactive). The mode supported in the first version is 01. Terminal count registers is only for HW measuring as the status is available in one DMA cycle only and no latching capability is available in this register. See section 4.3.5.3.

HiFn9710 or 9711 must be powered with 5.0Volt.

4.2.12 RAM

History buffer for compression unit. Applying SRAM sets maximum decompression performance to 15Mbytes/second.

4.2.13 EN/DECRYPTION & HASHING COMPONENT (EDHC)

Includes:

- DES and triple-DES encryption and decryption processor w/CBC.
- MD5 hash processor.
- Padding.
- Support for MD5-HMAC.

The interface to the LOCAL BUS implements:

- 32 bit data path.
- 9-bit address for internal register file.
- Reset control.
- Interrupt signaling.

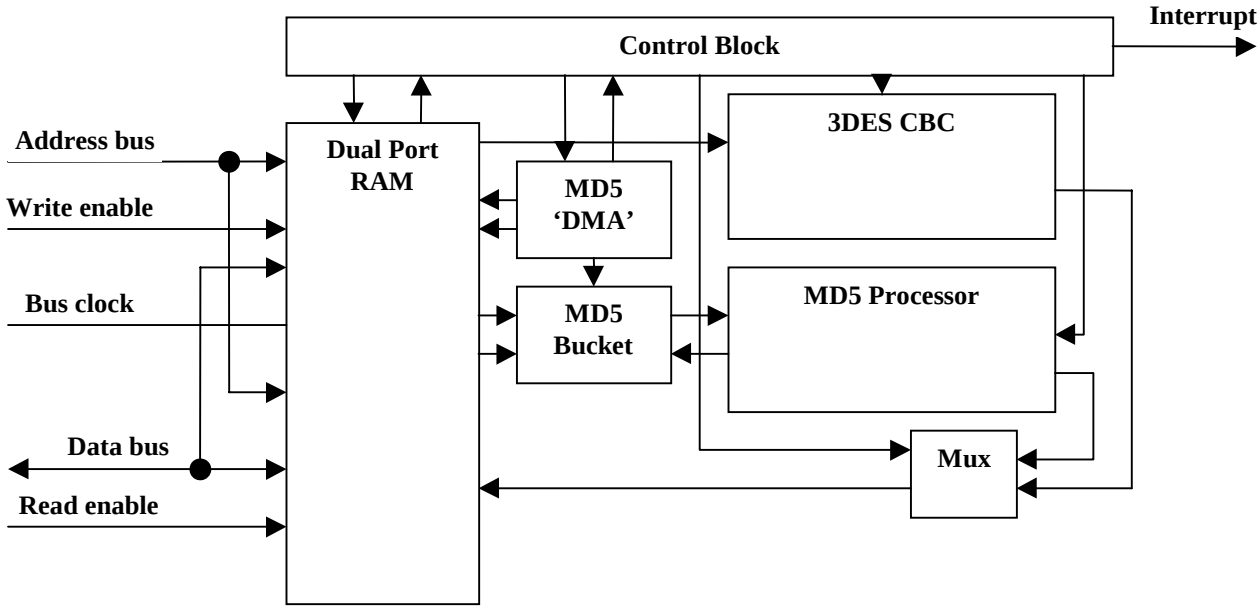
Inside this device:

- Register file based command interface.
- 2Kbyte of dual-port RAM for data buffering before data processing.
- 2Kbyte of dual-port RAM for data buffering after processing.
- DES and triple DES processor.
- Registers holding three keys.
- Register for control of CBC mode.
- Register for control of data type (cipher-, plain-text).
- CBC IV register.
- Padding insertion/extraction.
- MD5 processor.
- Register for control of MD5 process (on/off).
- Offset register for buffer start to DES processing start.

The order of actions to be taken for a data buffer to be processed will then be as follows:

1. Copy data to EDHC processor.
2. Await interrupt.
3. Copy data from EDHC processor

En/Decryption Hashing Device (EDHC) block diagram:



4.2.14 ISDN CONTROL

The PSB2115 (a single chip from Siemens) is selected to implement the ISDN Control function. This chip implements all necessary functions for an ISDN access solution. The LOCAL BUS interface is 8 bit data connected to bit 0 – 7, 8 address bit selecting internal registers and an interrupt signal.

It includes:

- An HDLC controller for the D-channel.
- Two protocol controllers for each B-channel.
- 2x64 bytes of FIFO per B-channel and per direction.
- A transceiver for the S-interface (Layer 1).

4.2.15 LINE I/F

Implements the physical interface to an ISDN subscriber line.

Includes:

- Line isolation
- S/T connector
- Conformance to CCITT I.430

4.2.16 PCI ARBITER

Will arbitrate for the PCI bus control on request from any master on the bus. When arbitration is done, it leaves control to the requesting part. Whenever 2 or more request bus control at the same time, a fairness arbitration scheme is applied. This means that if a master gets bus control it will be given lowest priority in a following arbitration, i.e. the priority will shift for each arbitration. This circuit will comply with PCI Specification rev 2.1.

4.2.17 HARDDISC CONTROLLER

The circuit is a PCI to IDE controller (one channel = 2 IDE devices) and a standard 40 pin IDE connector.
It will supports standard disk drivers.

4.2.18 ETHERNET CONTROLLER IC

Includes a 10/100 MAC controller with address filtering capabilities. A standard PCI interface and a DMA controller support transfers of data without CPU intervention. Further issues like auto-negotiation, promiscuous mode and LED control is available. The led control supports one Activity LED and one Link LED per controller. A MII interface sets signaling form to the LINE I/F.

4.2.19 ADDRESS FILTER

The Address Filter uses a table of MAC addresses to determine which frames to reject. This table is located in external local RAM, 32 Kbytes in size. Each MAC address in the table takes up 8 bytes (6 byte MAC + 2 bytes overhead, only 1 bit in the overhead is currently used).
The table is indexed by a 9-bit hash function giving space for 8 MAC addresses in each hash index. The hash function simply takes the 9 least significant bits from the MAC address and uses them as most significant bits in the table addressing.
The Address Filter can be set to one of two modes, the first is to reject all frames found in its table, the other is to only allow frames to pass if their address can be found in the table (Reject/Allow-mode).
The Address Filter determines if a received frame should be rejected by applying a hash function on its MAC address and search through 8 entries in the table at that hash index. If the address is found, the frame is either rejected or allowed to pass, depending on the mode of the Address Filter.

The Address Filter interfaces to the host CPU through the register file located in address 000h-003h. Through these locations the CPU can send commands to the Address Filter.
When a command has been carried out, a status message is generated. This message is either 0003h for success or 0002h for failure. If the status message is read before the command has finished, a value of 0000h will be read. There are two reasons why a command can fail:

1) No more free entries left in the table to carry out an insert-command.
2) An entry stated in a delete-command could not be found in the table.

4.2.20 MISC CIRCUITS

Includes the following circuits:

- 2 X 16 character LCD display
- LCD backlight power
- JTAG interface
- Fan power
- Board power connection
- Hard disc power

- PSU
- Initial boot prom interface
- Reset circuit
- Test

4.2.20.1 PSU

Specifications:
- 43W PSU giving 250V - 85V power connection
- 3,3V +/- 2% @ 4A
- 5,0 +/- 2%V @ 2A
- 12V +/- 5% @ 1,4A (2A peak for 15 sec)

4.2.20.2 Fan

Specifications:
- DC Brushless
- Max size : 40mm*40mm*10mm
- Operating Voltage: either 5V
- MTBF > 44000 hours

4.2.20.3 RESET CIRCUIT

Reset of all circuits is performed by a power monitor, and can be initiated by one of the following events:
- Whenever 3.3V or 5V powers up, or during operation if the voltage level falls below 3V respectively 4.65V. DS1834AS is a dual power supervisor from Dallas and is used in this circuit.
- "SYS" (system) button activated. To be able to trace a SYS button generated reset; a register flag is set whenever this reset source is previously detected. SW must clear this flag.
- Finally in system PLD programming enabled, will also activate reset.
- Sw controlled reset through a register

Reset of the processor is performed in 2 different levels: Cold Reset and Warm Reset. The Cold Reset causes the processor to be totally reinitialized. Termination of the cold reset phase indicates that the 3,3 and 5 V DC power and the MasterClock to have been stable for more than 350 ms. At this time the processor latches some basic configuration parameters (core clock multiplier, endianess, output driver strength, boot device width). The Warm Reset preserves the processor internal states. Causing internal processor state machines to be reset but preserves the contents in a number of internal registers. This feature enables some tracing to be performed, as a unique soft reset exception is executed after the warm reset. Furthermore SR bit in the processor status register will reflect this exception.

For the Processor below reset scheme is implemented:

Reset Source	Reset action
Power up or voltage drop	Cold Reset
PLD programming	Cold Reset
SYS Button	Cold Reset
Register controlled	Cold Reset

A cold reset cycle is always followed by a warm reset cycle. Warm reset only is not used in this implementation.
All reset sources will give full reset of any PCI device, the 79RC32134 and any 79RC32134 local bus peripheral.

The PCI-clock (33MHZ) will be running during reset.

4.2.20.4 TEST

One optional JTAG test connector is provided on the Board. The JTAG test chain is then routed between components supporting JTAG and further onto the PCI bus (according to PCI specification) to support JTAG on PCI and on any module.

On the main board following devices support JTAG:

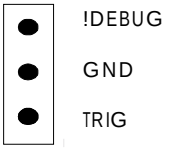
- Am79C972 Ethernet Controller
- MIPS processor (Cronus)
- System controller
- CPLD's and FPGA's
- Expansion slot

If a module inserted do not support JTAG, it can be bypassed (connecting TDI to the TDO signal) by inserting a jumper into a header. For any optional device included in the JTAG chain, such a bypass jumper is available. To do JTAG test, if the expansion slot is empty, the bypass jumper must also be inserted.

To support a provincial COM interface on the product even when the COM I/F is not mounted, a set of test points is given. They reveal the digital interface of the COM port, i.e. is the actual output signals of the system controller. In production test, the board specific test fixture must be able to connect to this interface and emulate a UART.

Test connectors provide easy logic analyzer measuring. The connectors used are 20 pin headers - HP Logic Analyzer type pin-layout. Signals found in the connectors are primarily CPU/System Controller signals for initial HW debug.

A 3 pin Debug/Trig connector is used to request the processor to enter a Debug program, after the execution of power on self-test. Connecting the !DEBUG pin to GND with a jumper directs the Processor to enter the Debug program. Leaving the !DEBUG pin unconnected makes the processor enter normal program execution. The !DEBUG signal is read by the Processor via a register. The third pin in the test connector provides a trigger output for debug purpose. The TRIG output is software controlled by a write to a register. See section 4.3.5.1



4.3 Memory map

The memory map base addresses are fully programmable by software. Base addresses must be set to define in which memory area the following device select signals are activated.

- BOOTCS(L) , boot device
- MEMCS0(L)
- MEMCS1(L)
- MEMCS2(L)
- MEMCS3(L)
- SDRAM_BCS0(L)
- SDRAM_BCS1(L)
- SDRAM_BCS2(L)
- SDRAM_BCS3(L)
- Internal Registers
- PCI I/O
- PCI Memory

Each of the device select signals will then enable resources/peripherals as shown in the table below.

Select line	Device/Resource	Bus Width/bits
BOOTCS(L)	Initial boot socket/On board flash	32
MEMCS0(L)	Compression device	32
MEMCS1(L)	Board Registers, ISDN devices, UART	32
MEMCS2(L)	En/Decryption, Hash device and Address Filter.	32
MEMCS3(L)	On board Flash	32
Internal Registers	GT64115 Internal Registers	32
PCI I/O	PCI I/O	32
PCI Memory	PCI Memory	32
SDRAM_BCS[1:0](L)	SDRAM	32
SDRAM_BCS[3:2](L)	Not Used	

Memory area's not defined by the setup of the system controller will generate a Bus error signal, leading to in a bus error exception.

Internal register control wait-state generation. To do a memory setup MEMCS1(L) must be set, then flash module presence is decoded, and now a full memory setup can be done. MEMCS1(L) must be defined as 32-bit memory, even though some registers will hold less valid data. For programming guidance on GT64115 internal registers see ref[2].

To do a memory setup for SDRAM_BCS0[1:0] the amount and size of sdram chips must be detected. In a one bank only configuration SDRAM_BCS0 selects all available sdram. In a two bank memory configuration SDRAM_BCS0 SELECTS bank 0 and SDRAM_BCS1 selects bank 1. In a two bank configuration, bank interleaving is possible. The table below will show what SDRAM_BCS0 signals to map as a function of the sdram chip size.

	64M bit Chips	128M bit Chips
SDRAM_BCS0	BANK0 = 16MByte	BANK0 = 32Mbyte
SDRAM_BCS1	BANK1 = 16MByte	BANK1 = 32MByte

SDRAM_BCS00 always select the first memory bank, SDRAM_BCS02 the second, SDRAM_BCS01 the third and finally SDRAM_BCS3 the last. But please note that each bank size differs.

4.3.1 Boot map configuration

A reset exception will always use the vector address BFC0.0000H. The System controller will then map this to BOOTCS(L) and put the address 1FC0.0000H on the address bus. BOOTCS(L) selects either boot sector in flash or "Initial Boot socket" inserted module as described previously.

4.3.2 PCI configuration map

For PCI configuration cycles following memory setup must be used:

Device	Configuration address
GT64115, System controller	8000.0000H
PCI0646, Hard Disk controller	4000.0000H
Am79c972, Ethernet 10/100 controller "IN"	2000.0000H
Am79c972, Ethernet 10/100 controller "OUT"	1000.0000H
Expansion Module	0800.0000H

The above map is given by connecting the msb address lines on the PCI bus to the IDSEL line on each of the PCI devices.

4.3.3 UART Registers

Is implemented by a 16550 with no control signals (only RXD and TXD). Detailed register definitions for this device can be found in the datasheets for the Texas TL16C550 device. The UART is selected by MEMCS1 with the offset address of 0x200000. Clock source for baud rate generation is 7.3728MHz.

4.3.4 Eeprom addressing

As previously explained the common eeprom interface implemented in the EEPROM_COMM register is used for access to the board id eeprom. The communication protocol is of standard I²C bus type. The device address is 1010000b

4.3.5 Board Registers, ISDN and UART

Will take up 4M byte address space. Individual registers are placed on 64K boundaries. The base address is defined by MEMCS1(L) memory setup. All registers are 16 or 8 bit wide outputting data on data-bit 15 to 0 respectively bit 7 to 0. Bit 31 to 16 are not valid. Within each 64K-address sector, any registers are then mirrored for each four bytes. Below is the address map with relative addresses

Rel. Address	**Name Read/write**	**Description Read/Write**
00000H – 0FFFFH	BOARD_CONT	Flash status/control, device reset control, initial boot status, System button control/status, test if.
10000H – 1FFFFH	EEPROM_COMM	Compression device interface select, eeprom's if control, and RTC if control.
20000H – 2FFFFH	DISPLAY	LCD display interface and compression device terminal count.
30000H – 3FFFFH	------	No registers implemented.
40000H – 4FFFFH	Soft Reset	Write only. When written a system reset (= cold boot) is generated.
50000H – 5FFFFH	FPGA Program Start	Write only. When written the FPGA enters program mode.
60000H – 6FFFFH	FPGA Program Stop	Write only. When written the FPGA leaves program mode.
70000H – 7FFFFH	------	No registers implemented
80000H – 8FFFFH	Interrupt status register	Interrupt sources
90000H – 9FFFFH	Interrupt mask register	Control of interrupt sources ability to activate common

		interrupt line
A0000H – AFFFFH	FPGA prg. Control/status	Control of FPGA programming cycle
B0000H – BFFFFH	UART controller	TL16550
C0000H – CFFFFH	ISDN controller	PSB2115
D0000H – FFFFFH	------	No registers implemented.

Each of the above registers will now be defined in details.

4.3.5.1 BOARD_CONT:

Default value = 0000.0000B
Data direction = Read/Write

Register	BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
Direction	R/W	R/W	R/W	R/W	R/W	R/W	R/*	R/*
Bit	DEBUG/ TRIG	ISDN_ RST	CRYPT_ RST	COMP_ RST	NOT_ USED	FL_ WEN	FL_ PRSNT	FL_ BUSY

DEBUG/TRIG **Debug jumper input or Trigger signal output**
Shows DEBUG jumper status when reading. Gives control of the TRIG output when writing.
Read
0: DEBUG jumper inserted
1: DEBUG jumper not inserted
Write
0: "0" on TRIG output
1: "1" on TRIG output

ISDN_RST **ISDN controller reset control**
0: Circuit is reset (value after boot).
1: Circuit is running

CRYPT_RST **En/Decryption + MD5 Hash processor reset control**
0: Circuit is reset (value after boot).
1: Circuit is running

COMP_RST **Compression module reset signal**
0: Compression module is reset (value after boot).
1: Compression module is running
Note: CMODE_B(1,0) must be initialized while module is reset.

NOT_USED **Do not control anything**
0: Register value is reset (value after boot).
1: Register value is set

FL_WEN **Flash Program Enable**
Enables/disables erase, programming on flash devices. When in disable state any write to flash memory is masked of.
0: disabled
1: enabled
Must also be set when programming/erasing the boot sector. See ref[6] for detailed information.

FL_PRSNT **Flash Module Present**
Shows if a flash module is inserted.

0: not inserted
1: inserted

* If written this bit controls a test led.
0: Test led on (default)
1: Test led off

FL_BUSY **Flash Status signal**
Is a wired or status signal, showing busy/ready state of the internal state machine of all flash devices.
0: Busy status from one or more flash devices
1: All devices shows ready state
See ref[6] for detailed information.

* If written this bit controls a test led.
0: Test led on (default)
1: Test led off

4.3.5.2 EEPROM_COMM:

Default value = 0000.0000B
Data direction = Read/Write

Register	BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
Direction	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	LAN2_X	LAN1_X	EE_ CS	EE_ DATA	EE_ SCLK	RTC_ RST	RTC_ DATA	RTC_ CLK

LAN(2,1)_X **LAN interface 2 or 1 cable crossed**
Configures the LAN connector for port respectively station connections. Swap the receive and transmit signal pairs.
0: connections as in station mode
1: connections as in port mode

EE_CS **Serial Eeprom Chip Select signal**
0: eeprom access is disabled
1: eeprom access is enabled
For signaling protocol and register definitions in eeprom see Atmel datasheets on 93C46.

EE_DATA **Eeprom Data signal**
For signaling protocol and register definitions in eeprom see 93C46 datasheets.
0: data signal low
1: data signal high

EE_SCLK **Serial Eeprom Clock signal**
For signaling protocol and register definitions in eeprom see 93C46.
0: Clock signal low
1: Clock signal high

RTC_RST **Real Time Clock Communication enable and synchronize**
For signaling protocol and register definitions see DALLAS Semiconductor datasheets on DS1603.
0: Communication disabled. Transition to 0 ends cycles and not completed cycles are terminated.
1: Communication cycle enabled. Transition to 1 initiates the start of a

communication cycle.

RTC_DATA **Real Time Clock Data signal**
For signaling protocol and register definitions see DALLAS Semiconductor datasheets on DS1603.
0: data signal low
1: data signal high and enabled for data input from RTC
Note: data must be written high to enable for reading RTC data.

RTC_CLK **Real Time Clock signaling**
For signaling protocol and register definitions see DALLAS Semiconductor datasheets on DS1603.
0: Clock signal low
1: Clock signal high

4.3.5.3 DISPLAY:

Default value = 0000.0000.0000.0000B
Data direction = Read/Write

Register	**BIT 15**	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 09**	**BIT 08**
Direction	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit	UEMPR2	UEMPR1	LED2	LED1	LED0	CD_RS	CD_RW	CD_E
Register	**BIT 07**	**BIT 06**	**BIT 05**	**BIT 04**	**BIT 03**	**BIT 02**	**BIT 01**	**BIT 00**
Direction	R/W	R/W	R/W	R/W	RW	R/W	R/W	R/W
Bit	CD_DB7	CD_DB6	CD_DB5	CD_DB4	CD_DB3	CD_DB2	CD_DB1	CD_DB0

UEMPR(2,1) **Universal Expansion Module Present**
Read
Besides from the "present" status of a PCI module these 2 signals will show the power requirements of the PCI module.
The bit combinations will give the following information:
00: PCI module present & maximum power consumption 7.5W
01: PCI module present & maximum power consumption 15W
10: PCI module present & maximum power consumption 25W
11: No PCI module present
See ref[6] for more information.

LED(2:0) **LED**
Controls the 3 LED's associated with the ISDN Interface.
0: LED is switched off
1: LED is switched on
Although these LED's are software controlled the suggested employment are:

LED2 :
LINK status shows that physical connection to the exchange is established. This bit can be written to as well as read.

LED1 :
CONNECT status shows that one or both B-channels have an active session. LED1 is a write only register.

LED0 :
ACTIVITY status shows that one or both B-channels are receiving or transmitting. LED0 is a write only register.

CD_RS **Character Display Register Select**
0: Command/Status
1: Data
See ref[8] for detailed information.

CD_RW **Character Display Read/Write**
Defines the direction of data to or from the display.
0: Write (data to be stored in display)
1: Read.
See ref[8] for detailed information.

CD_E **Character Display Enable**
Enables the character display for access.
0: Access disabled.
1: Access enabled.
See ref[8] for detailed information.

CD_DB(7:0) **Character Display Data Bit**
Holds the data to or from the character display. See ref[8] for detailed information.
See ref[8] for detailed information.

4.3.5.4 Soft Reset

Default value = not applicable.
Data direction = Write only

When written this register activates the System Reset signal. This signal is also activated at cold boot.
The value written to this register is “don’t care”

4.3.5.5 FPGA Program Start

Default value = not applicable.
Data direction = Write only

When written, this register will activate the FPGA Write signal and the FPGA Chip Select signal. These signals must be active during the entire program download period.

The value written to this register is “don’t care”.

4.3.5.6 FPGA Program Stop

Default value = not applicable.
Data direction = Write only

When written, this register will deactivate the FPGA Write signal and the FPGA Chip Select signal. When these signals are deactivated the FPGA is in operational mode.

The value written to this register is “don’t care”.

4.3.5.7 INTERRUPT STATUS:

Data direction = Read

Register	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
Direction								R
Bit	---	---	---	---	---	---	---	UART_ INT
Register	**BIT 07**	**BIT 06**	**BIT 05**	**BIT 04**	**BIT 03**	**BIT 02**	**BIT 01**	**BIT 00**
Direction	R	R	R	R	R	R	R	R
Bit	ISDN_ INT	CRY_ INT	COMP_ INT	UEM_ INT	HDC_ INT	ETH1_ INT	ETH2_ INT	GT_ INT

UART_INT **UART interrupt status**
0: not active
1: Active

ISDN_INT **ISDN Controller Interrupt status**
0: not active
1: Active

CRY_INT **CRYPTO and Filter FPGA Interrupt status**
0: not active
1: Active

COMP_INT **HIFN Compression device Interrupt status**
0: not active
1: Active

UEM_INT **PCI Expansion slot Interrupt status**
0: not active
1: Active

HDC_INT **Hard Disk Controller Interrupt status**
0: not active
1: Active

ETH1&2_INT **Ethernet Controllers Interrupt status**
0: not active
1: Active

GT_INT **GT64115 System Controller Interrupt status**
0: not active
1: Active

4.3.5.8 INTERRUPT MASK:

Default value = XXXX.XXX0.0000.0000B
Data direction = Read/Write

Register	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
Direction								R/W
Bit	---	---	---	---	---	---	---	UART_ MASK
Register	**BIT 07**	**BIT 06**	**BIT 05**	**BIT 04**	**BIT 03**	**BIT 02**	**BIT 01**	**BIT 00**
Direction	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	ISDN_ MASK	CRY_ MASK	COMP_ MASK	UEM_ MASK	HDC_ MASK	ETH1_ MASK	ETH2_ MASK	GT_ MASK

UART_MASK **UART interrupt mask control**
0: interrupt from this source disabled
1: interrupt enabled from this source

ISDN_ MASK **ISDN Controller interrupt mask control**
0: interrupt from this source disabled
1: interrupt enabled from this source

CRY_ MASK **CRYPTO and Filter FPGA interrupt mask control**
0: interrupt from this source disabled
1: interrupt enabled from this source

COMP_ MASK **HIFN Compression device interrupt mask control**
0: interrupt from this source disabled
1: interrupt enabled from this source

UEM_ MASK **PCI Expansion slot interrupt mask control**
0: interrupt from this source disabled
1: interrupt enabled from this source

HDC_ MASK **Hard Disk Controller interrupt mask control**
0: interrupt from this source disabled
1: interrupt enabled from this source

ETH1&2_ MASK **Ethernet Controllers interrupt mask control**
0: interrupt from this source disabled
1: interrupt enabled from this source

GT_ MASK **GT64115 System Controller interrupt mask control**
0: interrupt from this source disabled
1: interrupt enabled from this source

4.3.5.9 FPGA Control/Status:

Default value = 0000.0XX0B
Data direction = Read/Write

Register	BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
Direction	R	R	R	R	R	R	R	R/W
Bit	0	0	0	0	0	PRG_ INIT	PRG_ DONE	PROGRAM

PRG_INIT **Programming control/status of CRYPTO FPGA**
Shows the status of the FPGA clearing process to indicate when actual programming can start.
0: Ram clearing in progress
1: Ram clearing done (ready for program)

PRG_DONE **FPGA Programming done**
This register is a read only register. It shows the status of the programming cycle.
0: Programming in progress
1: Configuration load complete, Startup sequence in progress.

PROGRAM **Programming control/status of CRYPTO FPGA**
When written to it controls FPGA configuration. In fact it will control the PROGRAM(L) signal on the FPGA.
0: Initiates a FPGA configuration cycle
1: Terminates the configuration command
I.e. it must be pulsed low to start configuration.

4.4 Connector Definitions

4.4.1 Initial boot, Flash Module

Has a 72-pin dimm connector with the following pin-out.

Signal Name	Connector Pin No.	Signal Name	Connector Pin No.	Signal Name	Connector Pin No.
GND	1	---	25	---	49
A10	2	D0	26	D25	50
A5	3	---	27	D29	51
A21	4	A7	28	D24	52
GND	5	---	29	D30	53
D2	6	VCC	30	D23	54
A3	7	---	31	D31	55
A19	8	A6	32	D22	56
D9	9	A14	33	D32	57
D19	10	A11	34	D21	58
D10	11	A8	35	D33	59
#RD	12	#CS	36	D20	60
D11	13	GND	37	D34	61
D7	14	A18	38	D18	62
D12	15	A12	39	#WR	63
D6	16	A17	40	A4	64
D13	17	A13	41	PRSNT	65
D4	18	A16	42	VCC	66
D14	19	---	43	GND	67
D4	20	A9	44	---	68
D15	21	D27	45	---	69
D3	22	A20	46	A15	70
D16	23	D28	47	GND	71
D1	24	A2	48	GND	72

VCC = 3.3V

4.4.2 Module Connection

Is given by a Metric angled PCI, complying with PCI Revision 2.1. Power keying is set for 5V.

Connector Pin No.	Signal Name	Connector Pin No.	Signal Name	Connector Pin No.	Signal Name	Connector Pin No.	Signal Name
1A	#TRST	1B	-12V	32A	AD16	32B	AD17
2A	+12V	2B	TCK	33A	+3,3V	33B	#C/BE2
3A	TMS	3B	GND	34A	#FRAME	34B	GND
4A	TDI	4B	TDO	35A	GND	35B	#IRDY
5A	+5V	5B	+5V	36A	#TRDY	36B	+3,3V
6A	#INT	6B	+5V	37A	GND	37B	#DEVSEL
7A	--	7B	--	38A	#STOP	38B	GND
8A	+5V	8B	GND	39A	+3,3V	39B	#LOCK
9A	--	9B	S1	40A	GND	40B	#PERR
10A	+5V(I/O)	10B	GND	41A	S2	41B	+3,3V
11A	--	11B	--	42A	GND	42B	#SERR
12A	GND	12B	GND	43A	PAR	43B	+3,3V
13A	GND	13B	GND	44A	AD15	44B	#C/BE1
14A	--	14B	--	45A	+3,3V	45B	AD14
15A	#RST	15B	GND	46A	AD13	46B	GND
16A	+5V(I/O)	16B	CLK	47A	AD11	47B	AD12
17A	#GNT	17B	GND	48A	GND	48B	AD10
18A	GND	18B	#REQ	49A	AD09	49B	GND
19A	--	19B	+5V(I/O)	50A	CONN KEY	50B	CONN KEY
20A	AD30	20B	AD31	51A	CONN KEY	51B	CONN KEY
21A	+3,3V	21B	AD29	52A	#C/BE0	52B	AD08
22A	AD28	22B	GND	53A	+3,3V	53B	AD07
23A	AD26	23B	AD27	54A	AD06	54B	+3,3V
24A	GND	24B	AD25	55A	AD04	55B	AD05
25A	AD24	25B	+3,3V	56A	GND	56B	AD03
26A	IDSEL	26B	#C/BE3	57A	AD02	57B	GND
27A	+3,3V	27B	AD23	58A	AD00	58B	AD01
28A	AD22	28B	GND	59A	+5V(I/O)	59B	+5V(I/O)
29A	AD20	29B	AD21	60A	S3	60B	--
30A	GND	30B	AD19	61A	+5V	61B	+5V
31A	AD18	31B	+3,3V	62A	+5V	62B	+5V

Note: Minimum requirement for a module is 5V PCI interface and keying.

4.4.3 PSU Connection

14 Pin connector of Molex type 41791 or equivalent. Se pin-out below.

Signal Name	Connector Pin No.	Signal Name	Connector Pin No.
5V	1	3.3V	8
5V	2	GND	9
GND	3	3,3V	10
GND	4	12V *)	11
GND	5	GND *)	12
12V	6	GND *)	13
3,3V	7	5V *)	14

*) Used as output to supply the hard disc with power

4.4.4 Fan Connection

2 Pin connectors of Molex type 22-27-2021 or equivalent are used. Se pin-out below.

Connector	Signal Name
Pin No.	
1	5V
2	GND

4.4.5 Ethernet 10/100 UTP

Is an 8 pin shielded RJ45 connector. See pin-out below.

Signal Name	Connector	Signal Name	Connector
	Pin No.		Pin No.
TX+	1	TX_CMB	5
TX-	2	RX-	6
RX+	3	RX_CMA	7
TX_CMA	4	RX_CMB	8

4.4.6 BRI

Is an 8 pin shielded RJ45 connector. Pin-out below.

Signal Name	Connector	Signal Name	Connector
	Pin No.		Pin No.
--	1	TXD-/RING	5
--	2	RXD-/--	6
RXD+/--	3	--	7
TXD+/TIP	4	--	8

4.4.7 Debug port

Is a 6-pin header. See pin-out below.

Signal Name	Connector	Signal Name	Connector
	Pin No.		Pin No.
TXD_103	1	GND_102	4
RXD_104	2	RXD_104	5
GND_102	3	TXD_103	6

4.4.8 Lattice PLD programming interface

Is an 8-pin sil connector of AMP type 640452-8 or equivalent. Pin no 4 in this connector is left blank, to ensure that no polarization error will occur when connecting to the cable part.

Signal Name	Connector Pin No.	Signal Name	Connector Pin No.
SCLK	1	#ISPEN	5
GND	2	SDI	6
MODE	3	SDO	7
--	BLANK	VCC(5.0V)	8

4.4.9 LCD Backlight

2 Pin connectors of Molex type 22-27-2021 or equivalent are used. Se pin-out below.

Connector Pin No.	Signal Name
1	5V
2	GND

4.4.10 Hard Disc Connector

Is a 2x20 pin header. See pin-out below.

Connector Pin No.	Signal Name	Connector Pin No.	Signal Name
1	#RESET	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	N.C.
21	DMARQ	22	GND
23	#DIOW	24	GND
25	#DIOR	26	GND
27	IORDY	28	N.C.
29	#DMACK	30	GND
31	IRQ	32	N.C.
33	DA1	34	Pull Down (1Kohm)
35	DA0	36	DA2
37	CS0	38	#CS1
39	N.C.	40	GND

4.5 Mechanical Description

4.5.1 Design Constraints

The design constraints for the VPN BOX is given below:

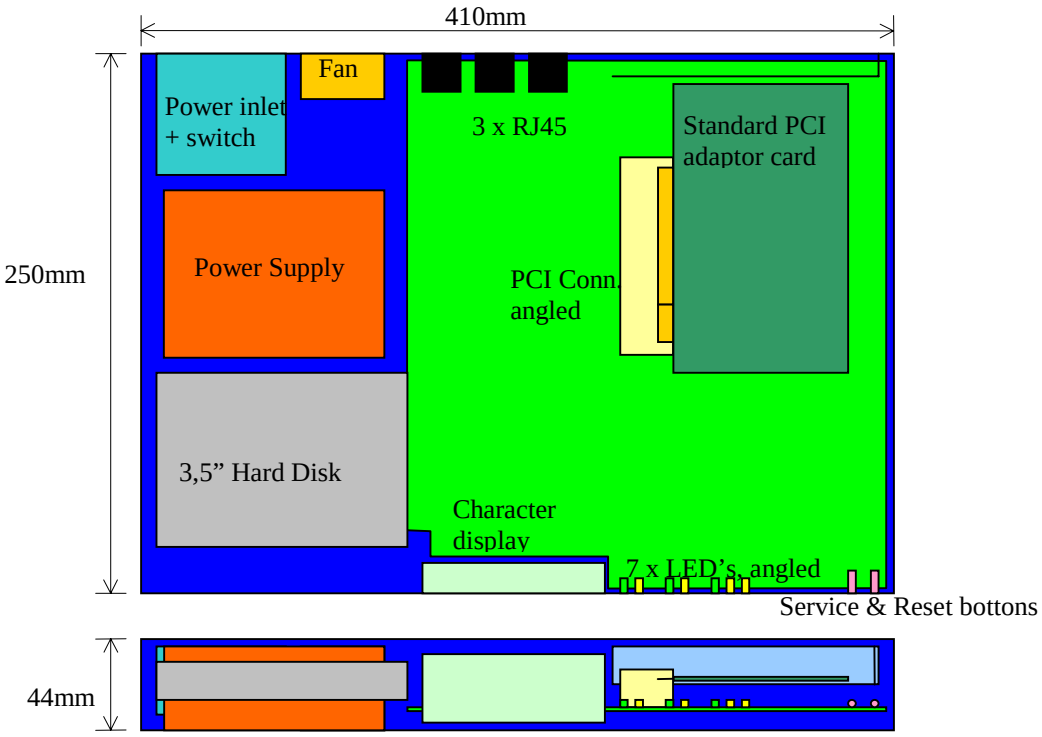
- The height of the box is 1U (approx. 44mm).
- Form factor for depth/length is 250mm/410mm
- Provision for 19" rack mounting.
- Esthetic design (i.e. an industrial designer is required).
- All cable attachment to the box is on the back
- One PCI slots for a standard PCI-card.
- Front bracket of the PCI card is accessible from the rear of the box.
- 3 RJ45 connectors for LAN and WAN connections on the rear.
- 7 LED's on the front showing "Link" and "Activity" for the 2 LAN connections and "Link", "Connect" and "Activity" for the WAN connection.
- "Link" LED's are green.
- "Activity" LED's are yellow.
- "Connect" LED is yellow.
- Push button for system reset. Accessible from the front through a hole in the front panel.
- Push button for Service Mode. Accessible from the front through a hole in the front panel.
- Character display (2 lines, each of 16 characters) on front.
- One 3,5" hard disc.
- Fan for cooling.
- EMC correct design.
- IEC Power Inlet with filter on the rear.
- Mains switch on the rear.
- Cabinet color is black.

4.5.2 Logo Definition

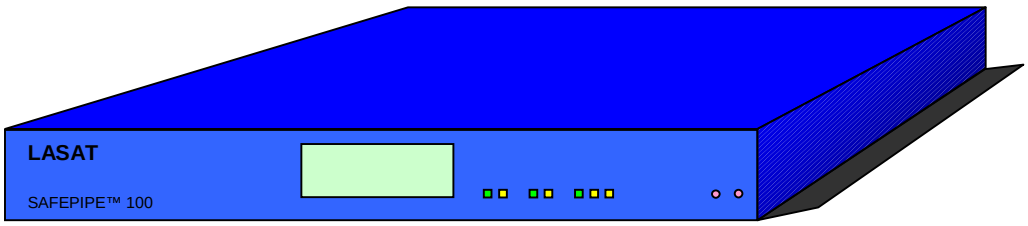
The logo used on cabinet is shown in the figure below:

4.5.3 The Box

A drawing of the VPN BOX is shown below. The drawing is not meant to a final design but rather a visualization of the various parameters, which have to be considered during the final design of the box.



Component planning for the box.



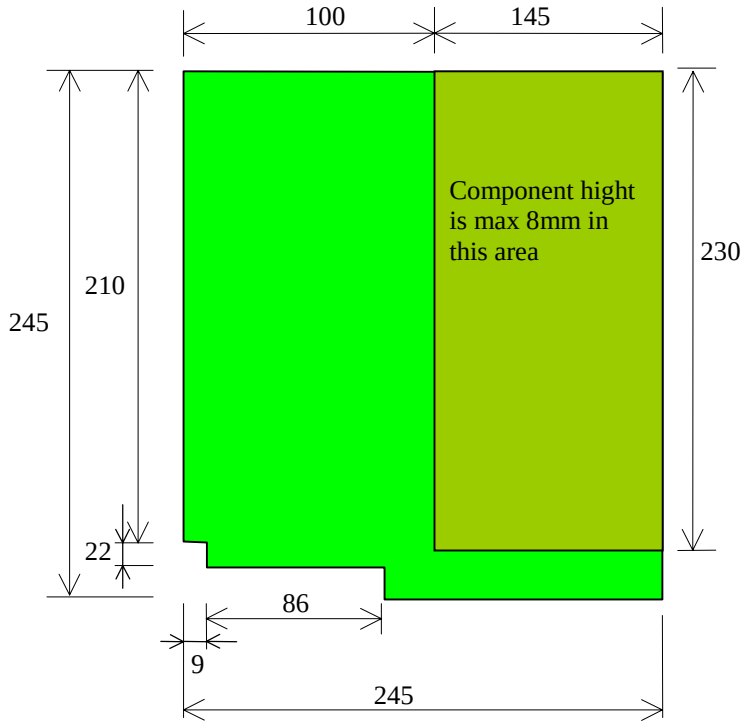
Front layout for the box

Logo text reads: ”LASAT”
Product name reads: ”SAFEPIPE™ 100”

4.5.4 PCB Outline

The figure below shows the PCB outline. The PCB will be 8 layers. 3 layers are dedicated to power distribution. Components are placed one side only.

The PCB must comply with i-data guidelines for PCB layout and manufacturing.



All dimensions in mm

4.6 Electrical Specifications

Parameter	Min	Typical	Max
Actual power figures, 3.3V		1.345A	
Actual power figures, 5V		0.395A	

4.7 Approvals and Compliance

4.7.1 ISDN Conformance

Primary target will be EURO ISDN layer 1 conformance. To support this, the top level regulative to address will be CTR3 released by European Telecommunication Standard Institute - ETSI. This regulative will present a hirachi that will define the ISDN BRI in details.

Hirachi level	Regulations
1	CTR3
2	TBR3 and Amendment (June 97)
3	ETS300012
4	I.430
5	ISO8877

Test report showing conformance to this is valid for all European countries:

To test conformance to above regulations the accredited approval department of TELE DANMARK will be used.

4.7.2 EMC

4.7.2.1 Electromagnetic Interference Performance

Electromagnetic Interference performance is tested with reference to the requirements showed below. The VPN Box, including all peripherals, must meet:

Region	Regulation, Shielded Cable	Regulation, Unshielded Cable
Europe	EN55022, Class B	EN55022, Class A
North America	FCC, part 15, subpart B Class B.	FCC, part 15, subpart B Class A.
Japan	VCCI class B	VCCI class A
Other	CISPR 22, Class B	CISPR 22, Class A

4.7.2.1.1 Power Line Harmonic Distortions

Comply with IEC 1000-3-2.

4.7.2.2 Electromagnetic Susceptibility Performance

Compliance to EN50082-1, incl. normative and informative annex, or EN55024.

4.7.3 Product Environment

4.7.3.1 Temperature and Humidity Environment

Product Power On :

Dry Bulb Temperature :	10 to 40 deg. C
Relative Humidity :	8 to 80 % non condensing
Wet Bulb Temperature :	27 deg. C

Product Power Off :

Dry Bulb Temperature :	10 to 52 deg. C
Relative Humidity :	8 to 80 % non condensing
Wet Bulb Temperature :	27 deg. C

Note :Assuming laminar air flow in area of card, the cooling capabilities of the chassis when in operating configuration shall not allow the air ambient box temperature to exceed 70 deg. C.

4.7.3.2 Altitude

0 to 3000 meters corresponding to the absolute pressure of 106 KPa down to 70 KPa.

4.7.3.3 Storage and Shipment Environment

Storage:

Dry Bulb Temperature:	1 to 60 deg. C
Relative Humidity:	5 to 80 %
Wet Bulb Temperature :	29 deg. C

Shipment:

Dry Bulb Temperature :	-40 to 60 deg. C
Relative Humidity :	5 to 100 %
Wet Bulb Temperature:	29 deg. C

4.7.3.4 Vibration and Shock Requirements

While placed in the retail package the VPN Box shall undergo a free fall test as specified below. No damages or functional failures must be observed after the test.

Free fall Test:
The test is performed according to IEC 68-2-32, Test Ed, Free Fall, specified as follows:

Height of Fall	:	0.6 to 1.2m
Number of falls	:	12, two in each attitude as given below
Test Surface	:	Concrete
Fall Sequencing	:	One fall on each side

4.7.4 Product Marking and Labeling

Product Marking consists of a Bar-code Label with serial number and product ID.
Product approvals and marking of:

- C-UL
- CE
- CE-according to Tele terminal directive.
- BABT approval

is also required.

4.7.5 Safety requirements

1. IEC 950:Latest Edition - Safety of Information Technology Equipment, Including Electrical Business Equipment.
2. UL 1950, Latest Edition.
3. CSA Standard CAN/CSA-C22.2 No. 950 - Safety of Information Technology Equipment, Including Electrical Business Equipment

EN 60950:Latest edition (CENELEC country deviations to IEC 950).

4.8 HW Cost Analysis (Preliminary)

Note: This is the initial cost analysis. Please refer to Purchase Manager for an updated cost analysis.

The estimated cost for the hardware is:

- VPN Box with compression, en/decryption and address filter: 430 USD
- Masquerade with hard disc 452 USD

Cost Breakdown for the VPN BOX:

Function	Description	Qty.	Std.Price	Per	total
Basic electronic:	Vr4310-133 CPU	1	17	1	17
	GT-64115 SYSTEM CONTROLLER	1	21	1	21
	LATTICE ISPLSI2032 PLD (PCI ARBITOR)	1	2	1	2
	FLASH 32Mbit (2M*16bit)	2	8,5	1	17
	SDRAM MODULE 16Mbyte 168 PIN	1	20	1	20
	CONNECTOR 168P DIMM (SDRAM)	1	2	1	2
	REAL TIME CLOCK (RTC)	1	4,5	1	4,5
	CONNECTOR 72P DIMM (INIT. BOOT SOCKET)	1	2	1	2
	EEPROM 2K SERIAL 2-W SO8, AT24C02N-10	1	0,4	1	0,4
	ISPLSI2032 (glue logic)	3	2,5	1	7,5
	SWITCH PUSHBUTTON SPST	1	0,15	1	0,15
	MISC. (Res., Cap, Diodes, Trans, etc)	1	5	1	5
	MAIN BOARD PCB, 6Layer	1	30	1	30
	SUPPLY SUPERVISOR 4.63V MAX809 SOT23	1	0,35	1	0,35
	SUPPLY SUPERVISOR 2.93V MAX809 SOT23	1	0,35	1	0,35
Ethernet:	AMD 79C792 PCI 10/100 ETH CNT.	2	13	1	26
	BCM5201 PHY 100BTX/FX/10BT MII TQFP64	2	5,5	1	11
	CRYSTAL 20MHz 20pF 20/F 50/T HC49S	2	0,5	1	1
	OSCILLATOR 25MHz 100PPM 40/60	2	0,96	1	1,92
	TANTAL 10uF 16V 20% H2.4 SMDB	14	0,12	1	1,68
	CERAMIC 15p 50V 5% NP0 0805	4	1,2	100	0,048
	CERAMIC 22n 50V +80/-20% Y5V 0603	80	0,8	100	0,64
	CERAMIC 27p 50V 5% NP0 0603	4	3,5	100	0,14
	CERAMIC 47p 50V 5% NP0 0603	2	1,3	100	0,026
	RESIST. 75R 1/4W 5% 1206	4	0,4	100	0,016
	RESIST. 1K 1/16W 5% 0603	40	0,4	100	0,16
	RESIST. 9K53 1/16W 1% 0603	2	0,01	1	0,02
	RESIST. 10R5 1/10W 1% 0805	6	0,7	100	0,042

	CONN. 8P. PHONE SHIELDED 8/8	2	0,28	1	0,56
	TRANSFORMER 10/100B-TX F.ML6692 SMD16	2	1,7	1	3,4
	FERRITE FILT WIDE 600R/100MHZ 200mA 0805	6	6,6	100	0,396
	INDUCTOR 330nH 20% 1210	4	0,14	1	0,56
	LED GREEN 3mm ANGLE M=1	2	0,2	1	0,4
	LED YELLOW 3mm ANGLE M=1	2	0,2	1	0,4
Address Filter:	SRAM 32K*8 20NS 3.3V	1	0,9	1	0,9
	EPLD XC95144 144MC 133I/O 10NS PQFP160	1	15	1	15
Expansion Slot:	CONN. 2*60P. PCI 32-bit RA 3.3V	1	6,95	1	6,95
	Blind plate	1	0,8	1	0,8
Compression:	COMPRESSION (HIFN9710)	1	23	1	23
	DRAM 256K*16	2	2	1	4
En/Decryption	FPGA 50K Gates	1	55	1	55
ISDN I/F:	ISDN COMM. CONTROLLER (PSB21525)	1	6	1	6
	BRI D-CH CONT. + ST-XCVR (PSB21866)	1	5	1	5
	ISPLSI1016, GLUE LOGIC	1	4,75	1	4,75
	CRYSTAL 15,36MHz 20pF 20/F 50/T HC49S	1	0,5	1	0,5
	LED YELLOW 3mm ANGLE M=1	2	0,2	1	0,4
	LED GREEN 3mm ANGLE M=1	1	0,2	1	0,2
	DIODE 1A 400V GF1 DO214BA	8	0,04	1	0,32
	DIODE 250mA 75V BAS16 SOT23	2	0,022	1	0,044
	TANTAL 10uF 10V 20% SMDB	8	0,1	1	0,8
	CERAMIC 22n 25V 10% X7R 0603	42	0,015	1	0,63
	RESISTORS 1/16W 5% 0603	40	0,0034	1	0,136
	RESISTORS 1/16W 1% 0603	30	0,0043	1	0,129
	INDUCTOR 330nH 10% 1008	10	0,15	1	1,5
	FERRITE FILTER 35R/100MHZ 200mA 0805	12	0,0606	1	0,7272
	ISDN ISOLATION TRANSFORMERS	1	2	1	2
	CONN. 8P. PHONE SHIELDED 8/8	1	0,28	1	0,28
Mechanics:	BOX	1	35	1	35
	FAN	1	5	1	5
	PSU	1	20	1	20
	POWER INLET W. FILTER	1	4	1	4
	POWER SWITCH	1	3	1	3
	Misc (Screws, Nuts, Gaskets, etc)	1	3	1	3
TOTAL:					376,7242
Overhead:	20% of cost price				71,7448
GRAND TOTAL					448,4690

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Cost Breakdown for the Masquerade configuration:

Function	Description	Qty.	Std.Price	Per	total
Basic electronic:	Vr4310-133 CPU	1	17	1	17
	GT-64115 SYSTEM CONTROLLER	1	21	1	21
	LATTICE ISPLSI2032 PLD (PCI ARBITOR)	1	2	1	2
	FLASH 32Mbit (2M*16bit)	2	8,5	1	17
	SDRAM MODULE 16Mbyte 168 PIN	1	20	1	20
	CONNECTOR 168P DIMM (SDRAM)	1	2	1	2
	REAL TIME CLOCK (RTC)	1	4,5	1	4,5
	CONNECTOR 72P DIMM (INIT. BOOT SOCKET)	1	2	1	2
	EEPROM 2K SERIAL 2-W SO8, AT24C02N-10	1	0,4	1	0,4
	ISPLSI2032 (glue logic)	3	2,5	1	7,5
	SWITCH PUSHBUTTON SPST	1	0,15	1	0,15
	MISC. (Res., Cap, Diodes, Trans, etc)	1	5	1	5
	MAIN BOARD PCB, 6Layer	1	30	1	30
	SUPPLY SUPERVISOR 4.63V MAX809 SOT23	1	0,35	1	0,35
	SUPPLY SUPERVISOR 2.93V MAX809 SOT23	1	0,35	1	0,35
Ethernet:	AMD 79C792 PCI 10/100 ETH CNT.	2	13	1	26
	BCM5201 PHY 100BTX/FX/10BT MII TQFP64	2	5,5	1	11
	CRYSTAL 20MHz 20pF 20/F 50/T HC49S	2	0,5	1	1
	OSCILLATOR 25MHz 100PPM 40/60	2	0,96	1	1,92
	TANTAL 10uF 16V 20% H2.4 SMDB	14	0,12	1	1,68
	CERAMIC 15p 50V 5% NP0 0805	4	1,2	100	0,048
	CERAMIC 22n 50V +80/-20% Y5V 0603	80	0,8	100	0,64
	CERAMIC 27p 50V 5% NP0 0603	4	3,5	100	0,14
	CERAMIC 47p 50V 5% NP0 0603	2	1,3	100	0,026
	RESIST. 75R 1/4W 5% 1206	4	0,4	100	0,016
	RESIST. 1K 1/16W 5% 0603	40	0,4	100	0,16
	RESIST. 9K53 1/16W 1% 0603	2	0,01	1	0,02
	RESIST. 10R5 1/10W 1% 0805	6	0,7	100	0,042
	CONN. 8P. PHONE SHIELDED 8/8	2	0,28	1	0,56
	TRANSFORMER 10/100B-TX F.ML6692 SMD16	2	1,7	1	3,4
	FERRITE FILT WIDE 600R/100MHZ 200mA 0805	6	6,6	100	0,396
	INDUCTOR 330nH 20% 1210	4	0,14	1	0,56
	LED GREEN 3mm ANGLE M=1	2	0,2	1	0,4
	LED YELLOW 3mm ANGLE M=1	2	0,2	1	0,4
Expansion Slot:	CONN. 2*60P. PCI 32-bit RA	1	6,95	1	6,95
	BLIND PLATE	1	0,8	1	0,8
Hard Disc:	PCI to IDE Hard Disc Controller Chip	1	7	1	7
	3,5" HARD DISC 4GBYTE	1	100	1	100
	Harddisc Interface accessories	1	1	1	1
ISDN I/F:	ISDN COMM. CONTROLLER (PSB21525)	1	6	1	6
	BRI D-CH CONT. + ST-XCVR (PSB21866)	1	5	1	5
	ISPLSI1016, GLUE LOGIC	1	4,75	1	4,75

	CRYSTAL 15,36MHz 20pF 20/F 50/T HC49S	1	0,5	1	0,5
	LED YELLOW 3mm ANGLE M=1	2	0,2	1	0,4
	LED GREEN 3mm ANGLE M=1	1	0,2	1	0,2
	DIODE 1A 400V GF1 DO214BA	8	0,04	1	0,32
	DIODE 250mA 75V BAS16 SOT23	2	0,022	1	0,044
	TANTAL 10uF 10V 20% SMDB	8	0,1	1	0,8
	CERAMIC 22n 25V 10% X7R 0603	42	0,015	1	0,63
	RESISTORS 1/16W 5% 0603	40	0,0034	1	0,136
	RESISTORS 1/16W 1% 0603	30	0,0043	1	0,129
	INDUCTOR 330nH 10% 1008	10	0,15	1	1,5
	FERRITE FILTER 35R/100MHZ 200mA 0805	12	0,0606	1	0,727
	ISDN ISOLATION TRANSFORMERS	1	2	1	2
	CONN. 8P. PHONE SHIELDED 8/8	1	0,28	1	0,28
Mechanics:	BOX	1	35	1	35
	FAN	1	5	1	5
	PSU	1	20	1	20
	POWER INLET W. FILTER	1	4	1	4
	POWER SWITCH	1	3	1	3
	Display 2*16 characters	1	8	1	8
	Misc (Screws, Nuts, Gaskets, etc)	1	3	1	3
TOTAL:					394,8
Overhead:	20% of cost price				75,4
GRAND TOTAL					470,2

5. Test Specification

5.1 Design Verification Test

6 pieces of 20 pin connectors fitting a logic analyzer pots (ex. HP), are placed on the PCB connecting to the basic CPU bus (control signals included). Further derived essential control signaling will also be supplied. Smallest possible interaction to preferred PCB layout must be obtained in placing the 6 connectors. This interface will enable debugging of HW and SW implementations. The Molex type 5332/20-pin connector is suggested for this test interface.

5.2 Production Test

The PCB will have test points on almost every net which makes it possible to perform an In Circuit Test (ICT) of the board. Circuit design and PCB layout, must comply with ICT demands, i.e. issues like spacing, terminating free pins, etc. must be considered.

JTAG will optionally be supported.

5.3 Test Programs

During the Design Verification Test and Production Test various types of test programs will be needed. These test programs must have following functionality:

- TBD

6. Future Enhancements

The below functionality will be considered for future product enhancements

- Tamper proof Enclosure
- US-ISDN (U interface)
- Centronics interface
- Temperature sense